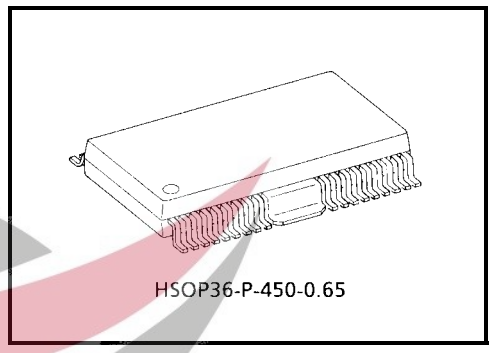
TOSHIBA Bi−CMOS Processor IC Silicon Monolithic

TB62202AF,TB62202AFG

Dual-Stepping Motor Driver IC for OA Equipment Using PWM Chopper Type

The TB62202AF/AFG is a dual-stepping motor driver driven by chopper micro-step pseudo sine wave.
To drive two-phase stepping motors, Two pairs of 16-bit latch and shift registers are built in the IC. The IC is optimal for driving stepping motors at high efficiency and with low-torque ripple.
The IC supports Mixed Decay mode for switching the attenuation ratio at chopping. The switching time for the attenuation ratio can be switched in four stages according to the load.



HSOP36-P-450-0.65

Weight: 0.79 g (typ.)

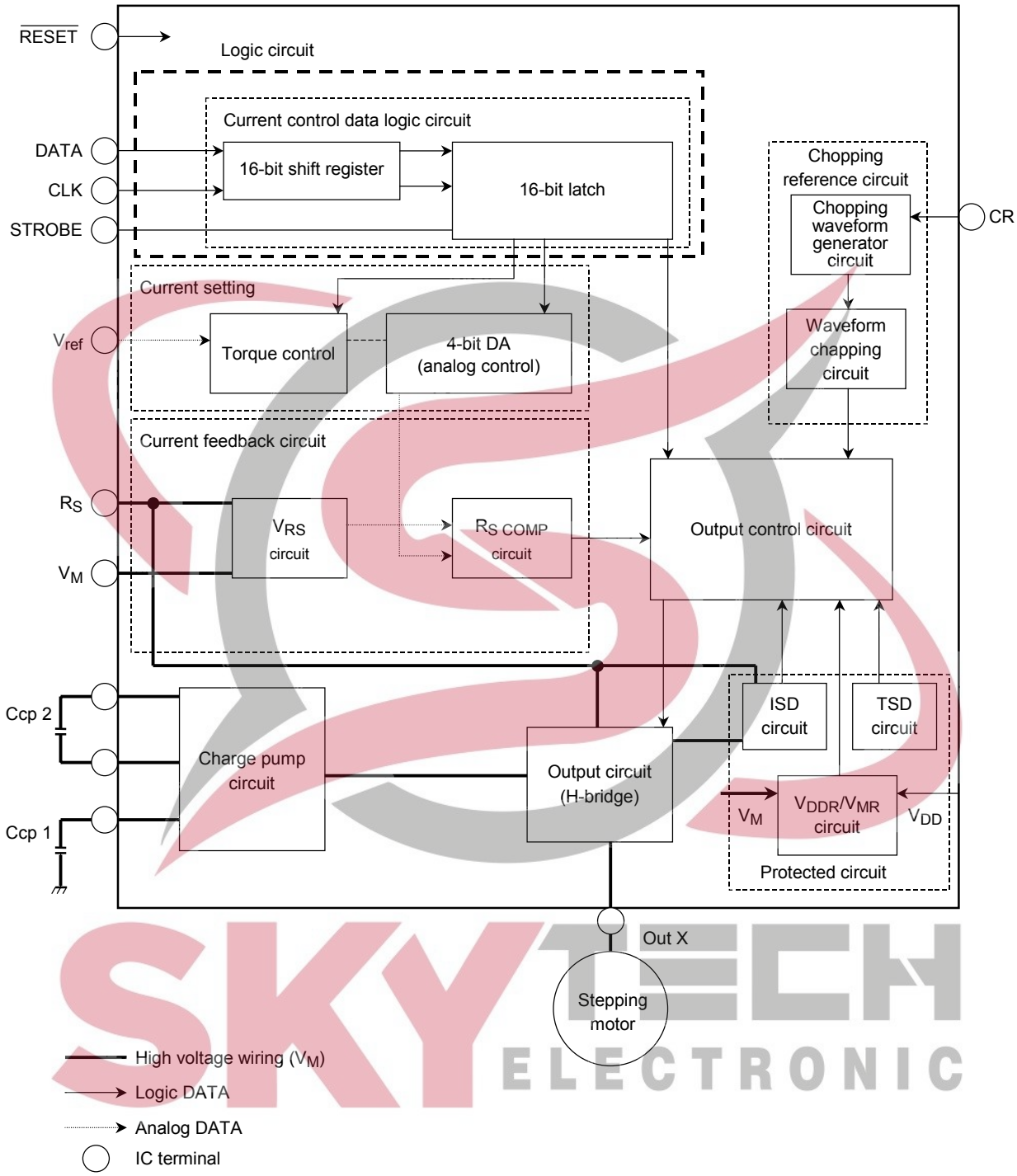
Features

- Two stepping motors driven by micro−step pseudo sine wave are controlled by a single driver IC
- Monolithic Bi-CMOS IC
- Low ON-resistance of Ron = 1.2 Ω (T_j = 25°C @1.0 A: Typ.)
- Two pairs of built-in 16-bit shift and latch registers
- Two pairs of built-in 4-bit DA converters for micro steps
- Built-in ISD, TSD, V_{DD} and V_M power monitor (reset) circuit for protection
- Built-in charge pump circuit (two external capacitors)
- 36-pin power flat package (HSOP36-P-450-0.65)
- Output voltage: 40 V max
- Output current: 1.0 A/phase max
- Built-in Mixed Decay mode enables specification of four-stage attenuation ratio. (The attenuation ratio table can be overwritten externally.)
- Chopping frequency can be set by external resistors and capacitors. High-speed chopping possible at 100 kHz or higher.

Note: When using the IC, pay attention to thermal conditions.
These devices are easy damage by high static voltage.
In regards to this, please handle with care.

Block Diagram

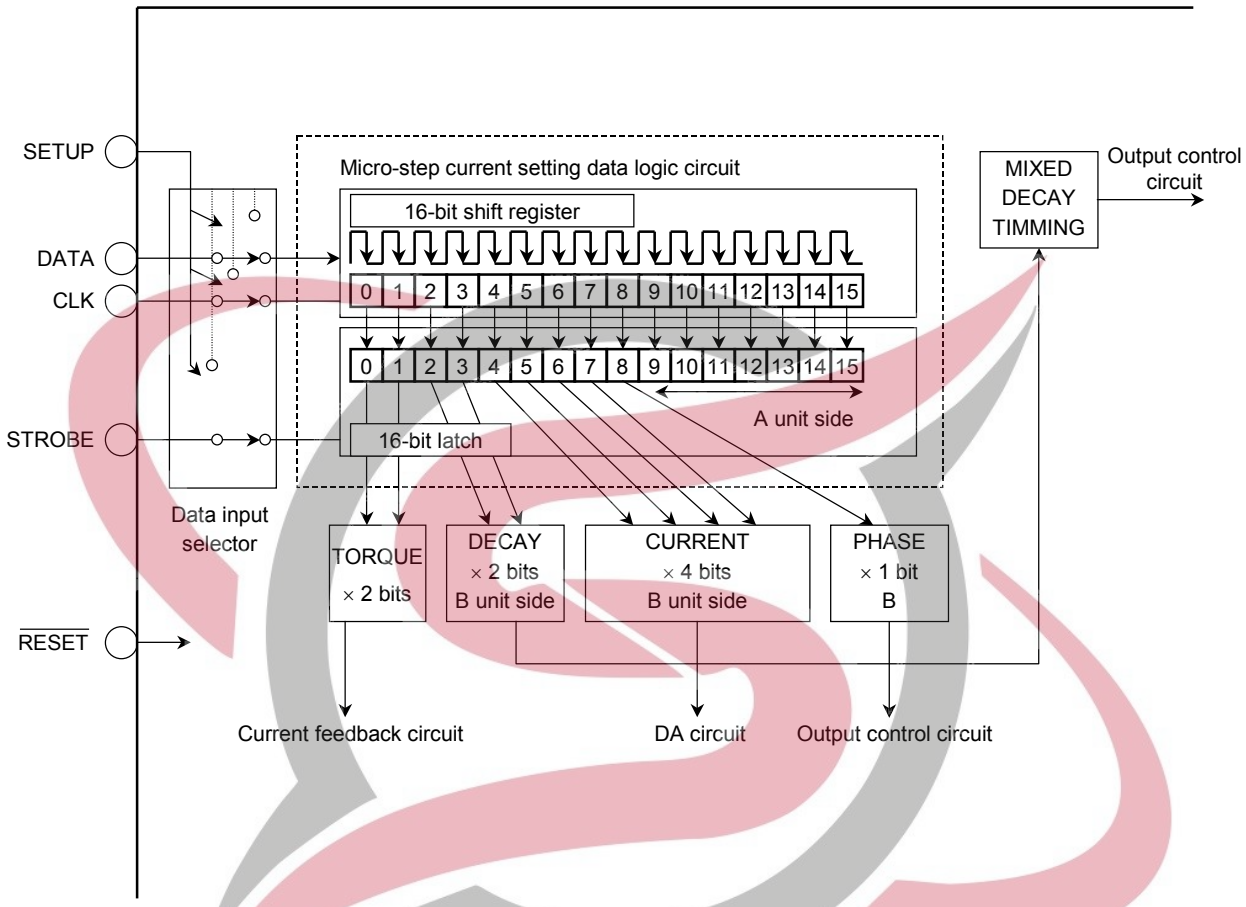
1. Overview (Power lines: A/B unit (C/D unit is the same as A/B unit))



2. Logic unit A/B (C/D unit is the same as A/B unit)

Function

This circuit is used to input from the DATA pins micro−step current setting data and to transfer them to the subsequent stage. By switching the SETUP pin, the data in the mixed decay timing table can be overwritten.

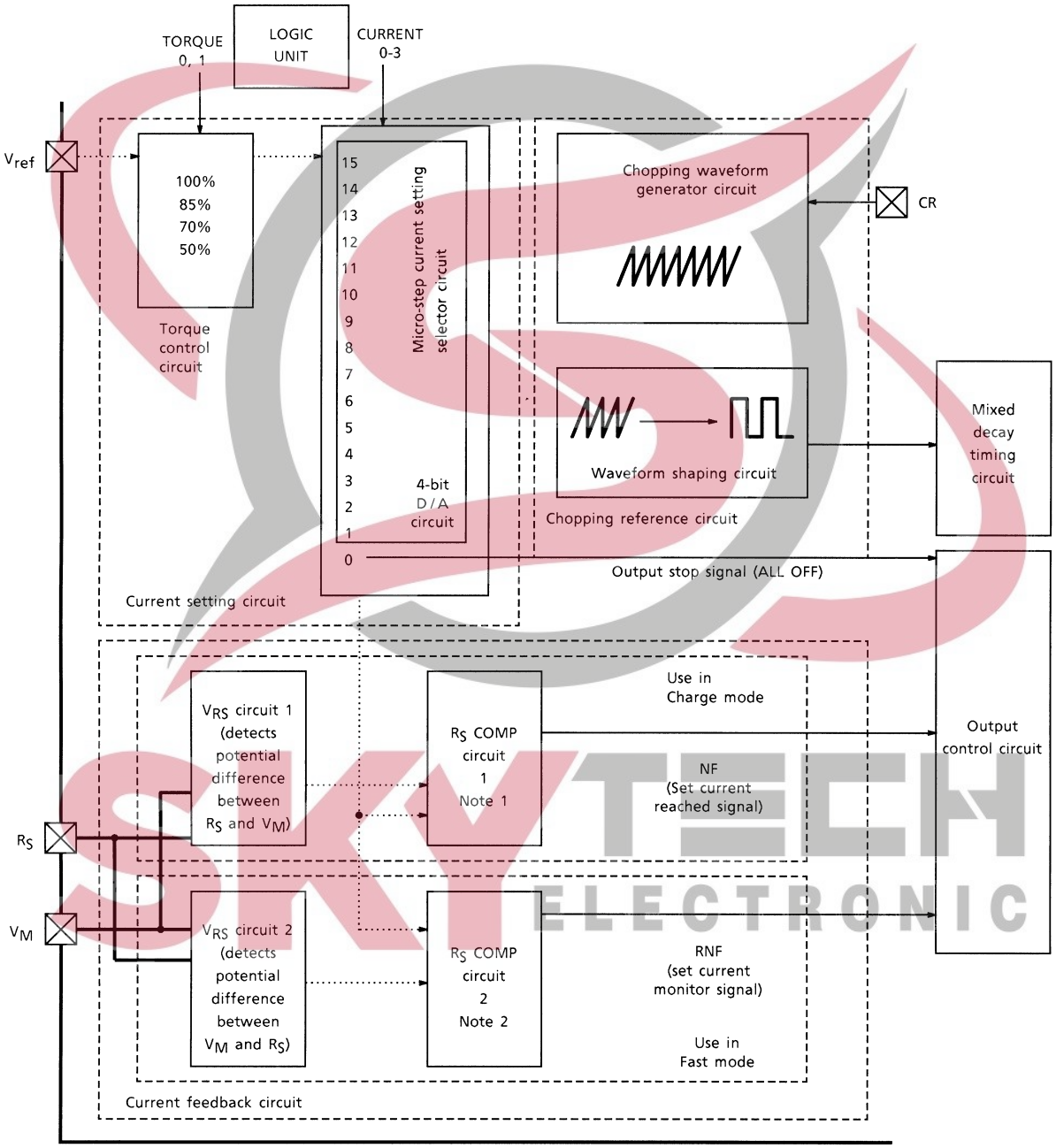


Note: The $\overline{\text{RESET}}$ and SETUP pins are pulled down in the IC by 10-kΩ resistor.
When not using these pins, connect them to GND. Otherwise, malfunction may occur.

3. Current feedback circuit and current setting circuit
(A/B unit (C/D unit is the same as A/B unit)

Function

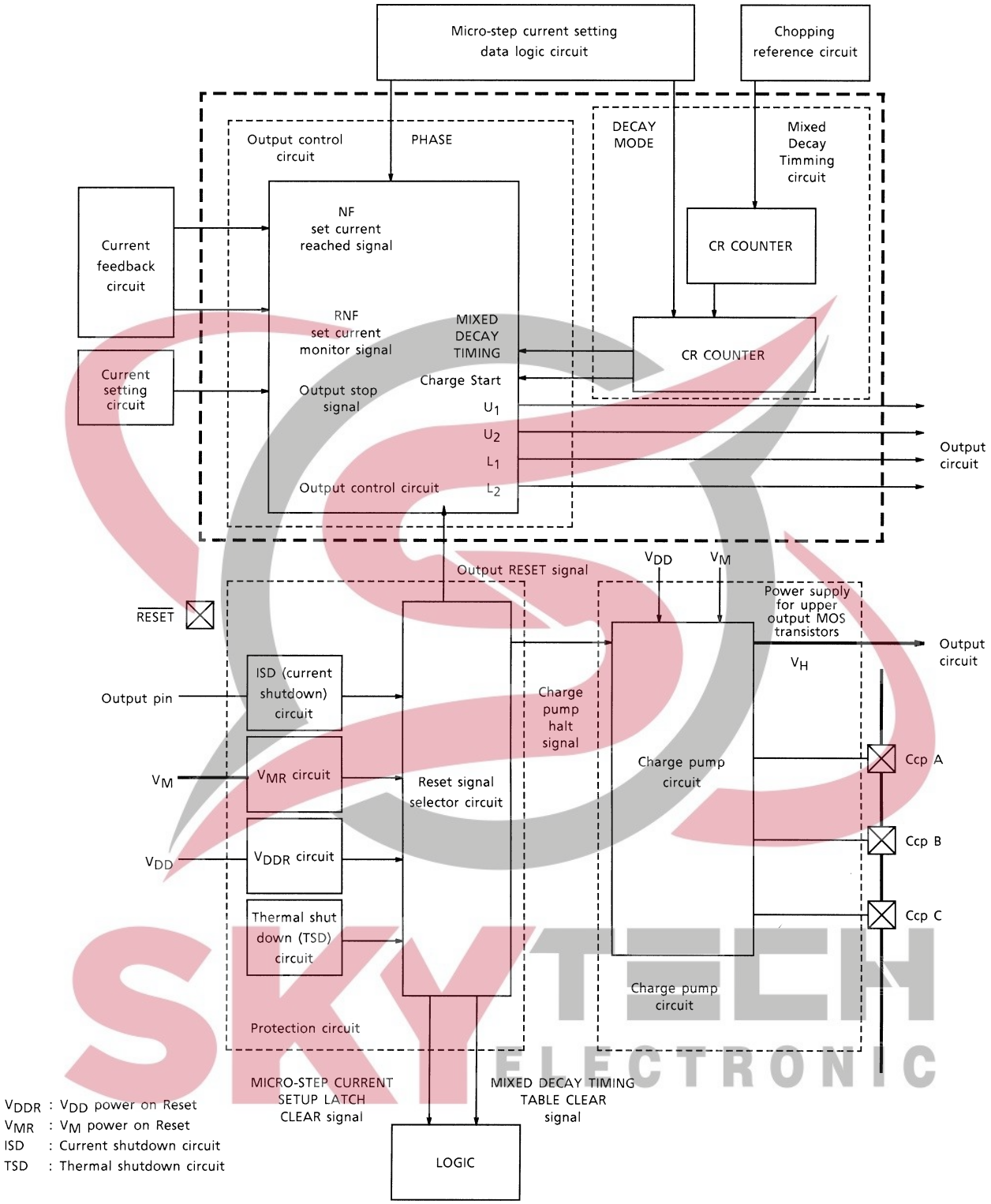
The current setting circuit is used to set the reference voltage of the output current using the micro−step current setting data input from the DATA pins.
The current feedback circuit is used to output to the output control circuit the relation between the set current value and output current. This is done by comparing the reference voltage output to the current setting circuit with the potential difference generated when current flows through the current sense resistor connected between RS and V_M.
The chopping waveform generator circuit to which CR is connected is used to generate clock used as reference for the chopping frequency.



Note 1: RS COMP 1: Compares the set current with the output current and outputs a signal when the output current reaches the set current.

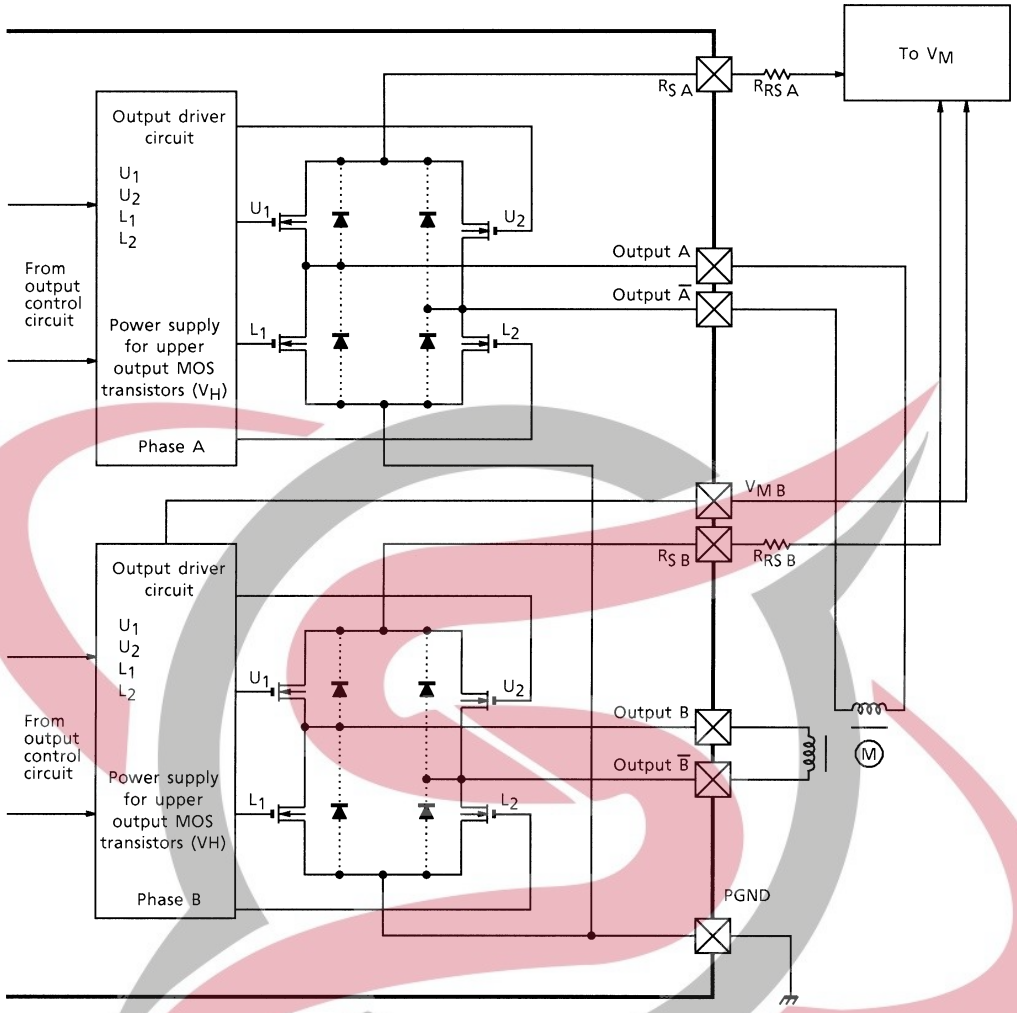
Note 2: RS COMP 2: Compares the set current with the output current at the end of Fast mode during chopping. Outputs a signal when the set current is below the output current.

4. Output control circuit, current feedback circuit and current setting circuit (A/B unit (C/D unit is the same as A/B unit)



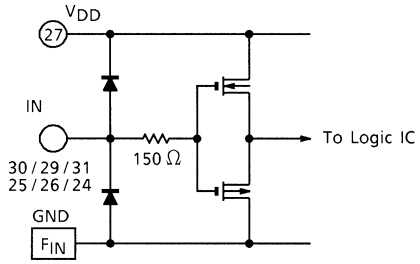
Note: The $\overline{\text{RESET}}$ pins is pulled down in the IC by 10-kΩ resistor.
When not using the pin, connect it to GND. Otherwise, malfunction may occur.

5. Output equivalent circuit (A/B unit (C/D unit is the same as A/B unit)

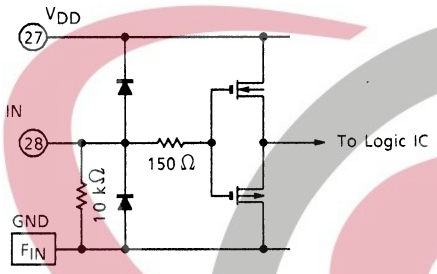


6. Input equivalent circuit

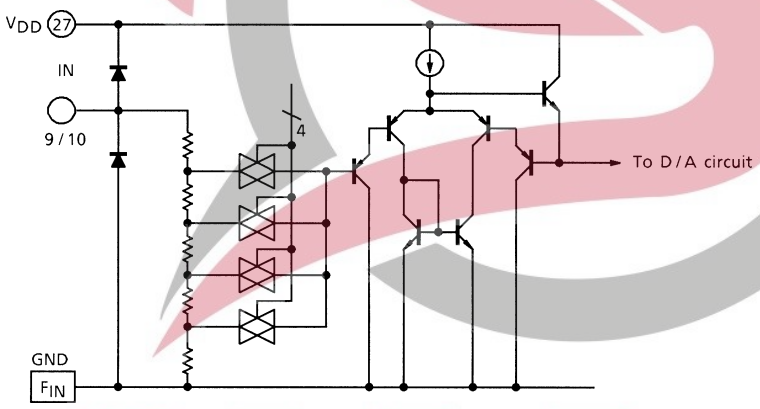
(1) Logic input circuit (CLK, DATA, STROBE)



(2) Input circuit ($\overline{\text{RESET}}$)

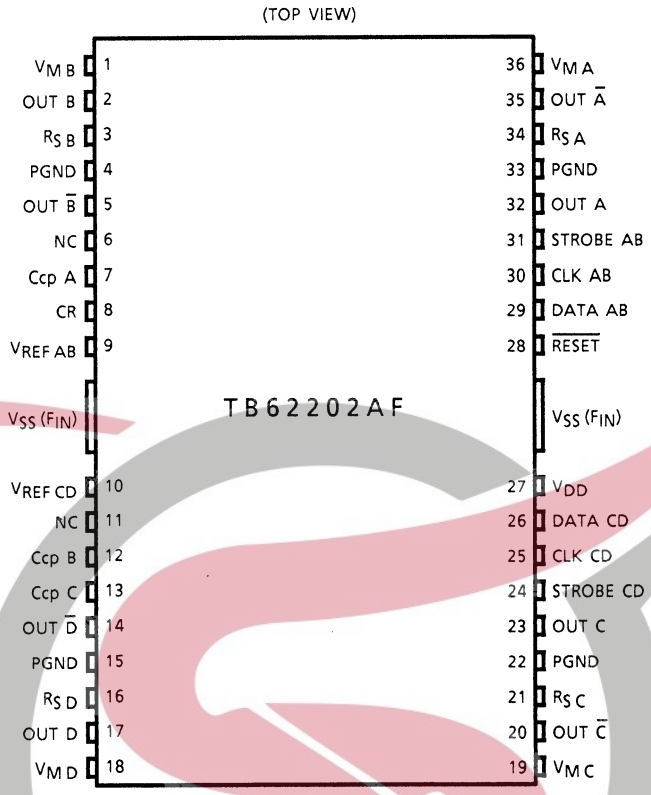


(3) V_{ref} input circuit



Note: $\overline{\text{RESET}}$ pin is pulled down. Do not use them open.
When not using these pins, connect them to GND.

Pin Assignment



Note: [Important] If this IC is inserted reverse, voltages exceeding the voltages of standard may be applied to some pins, causing damage.
Please confirm the pin assignment before mounting and using the IC.

Pin Description

Pin No.	Pin Symbol	Description
1	$V_{M\,B}$	Voltage major for output B block
2	OUT B	Output B pin
3	$R_{S\,B}$	Channel B current pin
4	PGND	Power GND pin
5	OUT $\overline{B}$	Output $\overline{B}$ pin
6	NC	Non connection
7	C_{cp} A	Capacitor pin for charge pump (Ccp1)
8	CR	External C/R (osc) pin (sets chopping frequency)
9	$V_{REF\,AB}$	V_{ref} input pin AB
F_{IN}	V_{SS}	F_{IN} (V_{SS}) : Logic GND pin
10	$V_{REF\,CD}$	Vref input pin CD
11	NC	Non connection
12	C_{cp} B	Capacitor pin for charge pump (Ccp2)
13	C_{cp} C	Capacitor pin for charge pump (Ccp2)
14	OUT $\overline{D}$	Output $\overline{D}$ pin
15	PGND	Power GND pin
16	$R_{S\,D}$	Channel D current pin
17	OUT D	Output D pin
18	$V_{M\,D}$	Voltage major for output D block
19	$V_{M\,C}$	Voltage major for output C block
20	OUT $\overline{C}$	Output $\overline{C}$ pin
21	$R_{S\,C}$	Channel C current pin
22	PGND	Power GND pin
23	OUT C	Output C pin
24	STROBE CD	CD STROBE (latch) signal input pin ($\sqcap$: LATCH)
25	CLK CD	CD clock input pin
26	DATA CD	CD serial data signal input pin
27	V_{DD}	Power pin for logic block
F_{IN}	V_{SS}	F_{IN} (V_{SS}) : Logic GND pin
28	$\overline{RESET}$	Output reset signal input pin (L : RESET)
29	DATA AB	AB serial data signal input pin
30	CLK AB	AB clock input pin
31	STROBE AB	AB STROBE (latch) signal input pin ($\sqcap$: LATCH)
32	OUT A	Output A pin
33	PGND	Power GND pin
34	$R_{S\,A}$	Channel A current pin
35	OUT $\overline{A}$	Output $\overline{A}$ pin
36	$V_{M\,A}$	Voltage major for output A block

Note: How to handle GND pins
All power GND pins and FIN (V_{SS}: signal GND) pins must be grounded.
Since FIN also functions as a heat sink, take the heat dissipation into consideration when designing the board.

Signal Functions

1. Serial input signals (for A/B. C/D is the same as A/B)

Data No.	Name	Functions
0 LSB	TORQUE 0	DATA No.0, 1 = HH: 100%, LH: 85%
1	TORQUE 1	HL: 70%, LL: 50%
2	DECAY MODE B_0	00: DECAY MODE 0, 01: DECAY MODE 1
3	DECAY MODE B_1	10: DECAY MODE 2, 11: DECAY MODE 3
4	Current B_0	Used for setting current. (LLLL = Output ALL OFF MODE) 4−bit current B data (Steps can be divided into 16 by 4−bit data)
5	Current B_1	
6	Current B_2	
7	Current B_3	
8	PHASE B	Phase information (H: OUT A: H, OUT $\overline{A}$: L)
9	DECAY MODE A_0	00: DECAY MODE 0, 01: DECAY MODE 1
10	DECAY MODE A_1	10: DECAY MODE 2, 11: DECAY MODE 3
11	Current A_0	Used for setting current. (LLLL = Output ALL OFF MODE) 4−bit current A data (Steps can be divided into 16 by 4−bit data)
12	Current A_1	
13	Current A_2	
14	Current A_3	
15 MSB	PHASE A	Phase information (H : OUT A : H, OUT $\overline{A}$: L)

(Note 1)

Note 1: Serial data input order
Serial data are input in the order LSB (DATA 0)
→ MSB (DATA 15)

Role of Data

Data Name	Number of Bits	Functions
TORQUE	2	Roughly regulates the current (four stages). Common to A and B units.
DECAY MODE	2 × 2 phases	Selects Decay mode. A and B units are set separately.
CURRENT	4 × 2 phases	Sets a 4−bit micro−step electrical angle. A and B units are set separately.
PHASE	1 × 2 phases	Determines polarity (+ or −). A and B units are set separately.

2. Serial input signal functions

Input						Action
CLK	STROBE	DATA	$\overline{RESET}$	VDDR (Note 1) or V_{MR}	Operation of TSD/ISD	(Note 2)
↑	×	×	H	H	L	No change in shift register.
↓	×	H	H	H	L	H level is input to shift register.
↓	×	L	H	H	L	L level is input to shift register.
×	↑	×	H	H	L	Shift register data are latched.
×	↓	×	H	H	L	Qn
×	×	×	L	×	L	Output off, charge pump halted (S/R DATA CLR)
×	×	×	×	L	L	Output off (S/R DATA CLR) Charge pump halted Mixed decay timing table cleared (only V_{DDR})
×	×	×	H	H	H	Output off (S/R DATA HOLD) Charge pump halted Restored when $\overline{RESET}$ goes from Low to High

×: Don't Care
Qn: Latched output level when STROBE is ↑.
Note 1: V_{DDR} and V_{MR}
H when the operable range (3 V typical) or higher and L when lower.
When one of V_{DDR} or V_{MR} is operating, the system resets (OR relationship).
Note 2: High when TSD is in operation.
When one of TSD or ISD is operating, the system resets (OR relationship).
Note: Function of overcurrent protection circuit
Until the RESET signal is input after ISD is triggered, the overcurrent protection circuit remains in operation.
During ISD, the charge pump stays halted.
When TSD and ISD are operating, the charge pump halts.

3. PHASE functions

Input	Function
H	Positive polarity (A: H, $\overline{A}$: L)
L	Negative polarity (A: L, $\overline{A}$: H)

4. DECAY mode X0, X1 functions

DECAY Mode X1	DECAY Mode X0	Function
L	L	Decay Mode 0 (Initial value: SLOW DECAY MODE)
L	H	Decay Mode 1 (Initial value: MIXED DECAY MODE: 37.5%)
H	L	Decay Mode 2 (Initial value: MIXED DECAY MODE: 75%)
H	H	Decay Mode 3 (Initial value: FAST DECAY MODE)

5. TORQUE functions

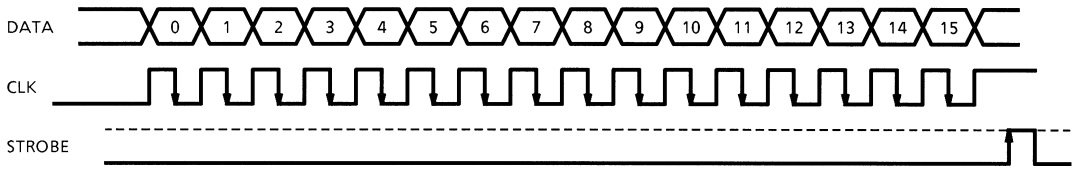
TORQUE 0	TORQUE 1	Comparator Reference Voltage Ratio
H	H	100%
L	H	85%
H	L	70%
L	L	50%

6. Current AX (BX) functions

Step	Set Angle	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
16	90.0	H	H	H	H	L	L	L	L
15	84.4	H	H	H	H	L	L	L	H
14	78.8	H	H	H	L	L	L	H	L
13	73.1	H	H	L	H	L	L	H	H
12	67.5	H	H	L	L	L	H	L	L
11	61.2	H	L	H	H	L	H	L	H
10	56.3	H	L	H	L	L	H	H	L
9	50.6	H	L	L	H	L	H	H	H
8	45.0	H	L	L	L	H	L	L	L
7	39.4	L	H	H	H	H	L	L	H
6	33.8	L	H	H	L	H	L	H	L
5	28.1	L	H	L	H	H	L	H	H
4	22.5	L	H	L	L	H	H	L	L
3	16.9	L	L	H	H	H	H	L	H
2	11.3	L	L	H	L	H	H	H	L
1	5.6	L	L	L	H	H	H	H	H
0	0.0	L	L	L	L	H	H	H	H

By inputting the above current data (A: 4-bit, B: 4-bit), 17-microstep drive is possible. For 1 step fixed to 90 degrees, see the section on output current vector line (85 page).

7. Serial data input setting



Note: Data input to the DATA pin are 16-bit serial data.
Data are transferred from DATA 0 (Torque 0) to DATA 15 (Phase A). Data are input and transferred at the following timings.
At CLK falling edge: data input
At CLK rising edge: data transfer
After data are transferred, all data are latched on the rising edge of the STROBE signal.
As long as STROBE is not rising, the signal can be either Low or High during data transfer.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit	
Logic supply voltage	V_{DD}	7	V	
Output voltage	V_M	40	V	
Output current	I_{OUT}	1.5	A/phase	(Note 1)
Current detect pin voltage	V_{RS}	$V_M \pm 4.5$	V	
Charge pump pin maximum voltage (CCP1 pin)	V_H	$V_M + 7.0$	V	
Logic input voltage	V_{IN}	to $V_{DD} + 0.4$	V	
Power dissipation	P_D	1.4	W	(Note 2)
		3.2	W	(Note 3)
Operating temperature	T_{opr}	−40 to 85	°C	
Storage temperature	T_{stg}	−50 to 150	°C	
Junction temperature	T_j	150	°C	

Note 1: Perform thermal calculations for the maximum current value under normal conditions. Use the IC at 1.2 A or less per phase.
Note 2: Input 7 V or less as V_{IN}.
Note 3: Measured for the IC only. (Ta = 25°C)
Note 4: Measured when mounted on the board. (Ta = 25°C)
Ta: IC ambient temperature
T_{opr}: IC ambient temperature when starting operation
T_j: IC chip temperature during operation T_j (max) is controlled by TSD (thermal shut down circuit)

Recommended Operating Conditions (Ta = 0 to 85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Power supply voltage	V_{DD}	—	4.5	5.0	5.5	V
Output voltage	V_M	V_{DD} = 5.0 V	20	24	34	V
Output current	$I_{OUT\ (1)}$	Ta = 25°C, per phase (when one motor is driven)	—	0.6	0.9	A
	$I_{OUT\ (2)}$	Ta = 25°C, per phase (when two motors are driven)	—	0.6	0.9	A
Logic input voltage	V_{IN}	—	GND	—	V_{DD}	V
Clock frequency	f_{CLK}	V_{DD} = 5.0 V	1.0	6.25	25	MHz
Chopping frequency	f_{chop}	V_{DD} = 5.0 V	40	100	150	KHz
Reference voltage	V_{ref}	V_M = 24 V, T_{orque} = 100%	2.0	3.0	V_{DD}	V
Current detect pin voltage	V_{RS}	V_{DD} = 5.0 V	0	±1.0	±1.5	V

Note: Use the maximum junction temperature (T_j) at 120°C or less

Electrical Characteristics 1
(Unless otherwise specified, Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input voltage	High	$V_{IN\ (H)}$	1	CLK, $\overline{RESET}$, STROBE, DATA pins	2.0	V_{DD}	V_{DD} + 0.4	V
	Low	$V_{IN\ (L)}$			GND − 0.4	GND	0.8	
Input current 1		$I_{IN1\ (H)}$	2	CLK, STROBE, DATA pins	—	—	1.0	μA
		$I_{IN1\ (L)}$			—	—	1.0	
Input current 2		$I_{IN2\ (H)}$		$\overline{RESET}$, SETUP pins	—	—	700	μA
		$I_{IN2\ (L)}$			—	—	700	
Power dissipation (V_{DD} pin)		I_{DD1}	2	V_{DD} = 5 V (STROBE, $\overline{RESET}$, DATA = L), $\overline{RESET}$ = L, Logic, output all off	—	3.0	6.0	mA
		I_{DD2}		Output OPEN, f_{CLK} = 6.25 MHz LOGIC ACTIVE, V_{DD} = 5 V, Charge pump = charged	—	4.0	8.0	
Power dissipation (V_M pin)		I_{M1}	3	Output OPEN (STROBE, $\overline{RESET}$, DATA = L), $\overline{RESET}$ = L, Logic, output all off Charge Pump = no operation	—	5.0	6.0	mA
		I_{M2}		Output OPEN, f_{CLK} = 6.25 MHz LOGIC ACTIVE, V_{DD} = 5 V, V_M = 24 V, Output off Charge Pump = charged	—	12	20	
		I_{M3}	4	Output OPEN, f_{CLK} = 6.25 MHz LOGIC ACTIVE, 100 kHz chopping (emulation), Output OPEN, Charge Pump = charged Ccp1 = 0.22 μF, Ccp2 = 0.01μf	—	30	40	
Output standby current	Upper	I_{OH}	5	$\overline{RS}$ = VM = 24 V, V_{out} = 0 V, $\overline{RESET}$ = H, DATA = ALL L	−400	—	—	μA
Output bias current	Upper	I_{OB}		$\overline{RS}$ = VM = 24 V, V_{out} = 24 V, $\overline{RESET}$ = H, DATA = ALL L	−200	—	—	
Output leakage current	Lower	I_{OL}		$\overline{RS}$ = VM = CcpA = V_{out} = 24 V, $\overline{RESET}$ = L	—	—	1.0	
Comparator reference voltage ratio	High (Reference)	$V_{RS\ (H)}$	6	V_{ref} = 3.0 V, V_{ref} (Gain) = 1/5.0 TORQUE = (H.H) = 100% set	—	100	—	%
	Mid High	$V_{RS\ (MH)}$		V_{ref} = 3.0 V, V_{ref} (Gain) = 1/5.0 TORQUE = (H.L) = 85% set	83	85	87	
	Mid Low	$V_{RS\ (ML)}$		V_{ref} = 3.0 V, V_{ref} (Gain) = 1/5.0 TORQUE = (L.H) = 70% set	68	70	72	
	LOw	$V_{RS\ (L)}$		V_{ref} = 3.0 V, V_{ref} (Gain) = 1/5.0 TORQUE = (L.L) = 50% set	48	50	52	
Output current differential		ΔI_{out1}	7	Differences between output current channels I_{out} = 1000 mA	−5	—	5	%
Output current setting differential		ΔI_{out2}	7	I_{out} = 1000 mA	−5	—	5	%
RS pin current		IRS	8	$\overline{VRS}$ = 24 V, V_M = 24 V, $\overline{RESET}$ = L (RESET status)	—	—	10	μA

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output transistor drain-source on-resistance	$R_{ON\ (D-S)\ 1}$	9	I_{out} = 1.0 A, V_{DD} = 5.0 V T_j = 25°C, Drain-source	—	1.1	1.3	Ω
	$R_{ON\ (D-S)\ 1}$		I_{out} = 1.0 A, V_{DD} = 5.0 V T_j = 25°C, Source-drain	—	1.1	1.3	
	$R_{ON\ (D-S)\ 2}$		I_{out} = 1.0 A, V_{DD} = 5 V, T_j = 105°C, Drain-source	—	1.4	1.6	
	$R_{ON\ (D-S)\ 2}$		I_{out} = 1.0 A, V_{DD} = 5 V, T_j = 105°C, Source-drain	—	1.4	1.6	

Electrical Characteristics 2
(Unless otherwise specified, Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
V_{ref} input voltage	V_{ref}	10	V_M = 24 V, V_{DD} = 5 V, $\overline{RESET}$ = H, Output on	2.0	—	V_{DD}	V
V_{ref} input current	I_{ref}	10	$\overline{RESET}$ = H, Output off V_M = 24 V, V_{DD} = 5 V, V_{ref} = 3.0 V	0	—	100	μA
V_{ref} attenuation ratio	V_{ref} (GAIN)	6	V_M = 24 V, V_{DD} = 5 V, $\overline{RESET}$ = H, Output on, V_{ref} = 2.0 to V_{DD} − 1.0 V	1/4.8	1/5.0	1/5.2	—
TSD temperature	T_jTSD (Note 1)	11	V_{DD} = 5 V, V_M = 24 V	130	—	170	°C
TSD return temperature difference	ΔT_jTSD	11	T_jTSD = 130 to 170°C	—	T_jTSD − 35	—	°C
V_{DD} return voltage	V_{DDR}	12	V_M = 24 V, $\overline{RESET}$ = H, STROBE = H	2.0	—	4.0	V
V_M return voltage	V_{MR}	13	V_{DD} = 5 V, $\overline{RESET}$ = H, STROBE = H	2.0	—	4.0	V
Over current protected circuit operation current	I_{SD} (Note 2)	14	V_{DD} = 5V, V_M = 24V, fchop = 100 kHz set	—	2.6	—	A

Note 1: Thermal shut down (TSD) circuit

When the IC junction temperature reaches the specified value and the TSD circuit is activated, the internal reset circuit is activated switching the outputs of both motors to off.

When the temperature is set between 130 (min) to 170°C (max), the TSD circuit operates. When the TSD circuit is activated, the function data latched at that time are cleared. Output is halted until the reset is released. While the TSD circuit is in operation, the charge pump is halted.

Even if the TSD circuit is activated and $\overline{RESET}$ goes H → L → H instantaneously, the IC is not reset until the IC junction temperature drops 35°C (typ.) below the TSD operating temperature (hysteresis function).

Note 2: Overcurrent protection circuit

When current exceeding the specified value flows to the output, the internal reset circuit is activated switching the outputs of both shafts to off.

When the ISD circuit is activated, the function data latched at that time are cleared.

Until the $\overline{RESET}$ signal is input, the overcurrent protection circuit remains activated.

During ISD, the charge pump halts.

For failsafe operation, be sure to add a fuse to the power supply.

Electrical Characteristics 3

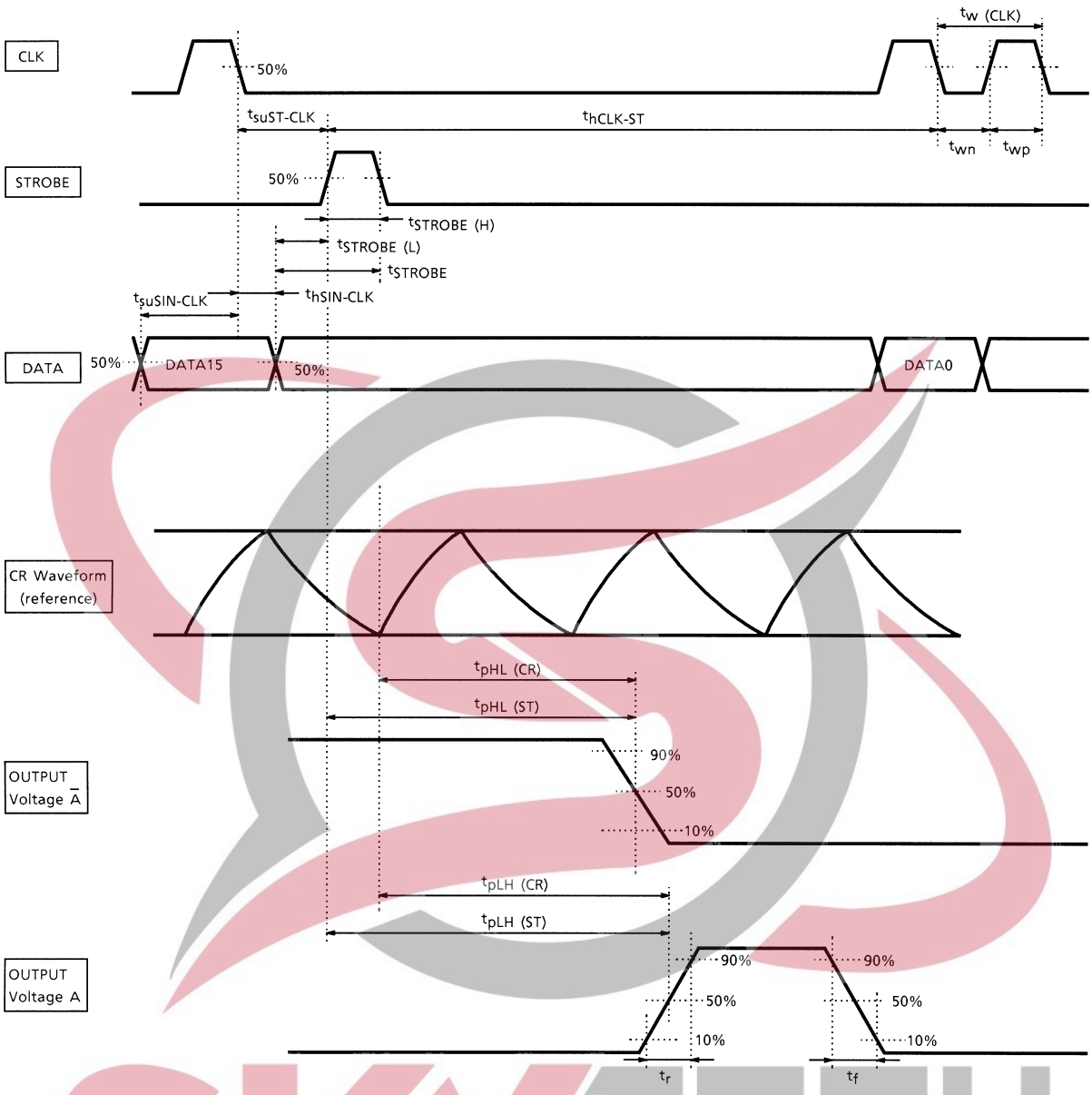
(Ta = 25°C, V_{DD} = 5 V, V_M = 24 V, I_{out} = 1.0 A)

Characteristics	SymboL	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Chopper current	Vector	15	θA = 90 (θ16)	—	—	100	—	%
			θA = 84 (θ15)		—	100	—	
			θA = 79 (θ14)		93	98	—	
			θA = 73 (θ13		91	96	—	
			θA = 68 (θ12)		87	92	97	
			θA = 62 (θ11)		83	88	93	
			θA = 56 (θ10)		78	83	88	
			θA = 51 (θ9)		72	77	82	
			θA = 45 (θ8)		66	71	76	
			θA = 40 (θ7)		58	63	68	
			θA = 34 (θ6)		51	56	61	
			θA = 28 (θ5)		42	47	52	
			θA = 23 (θ4)		33	38	43	
			θA = 17 (θ3)		24	29	34	
			θA = 11 (θ2)		15	20	25	
			θA = 6 (θ1)		5	10	15	
			θA = 0 (θ0)		—	0	—	

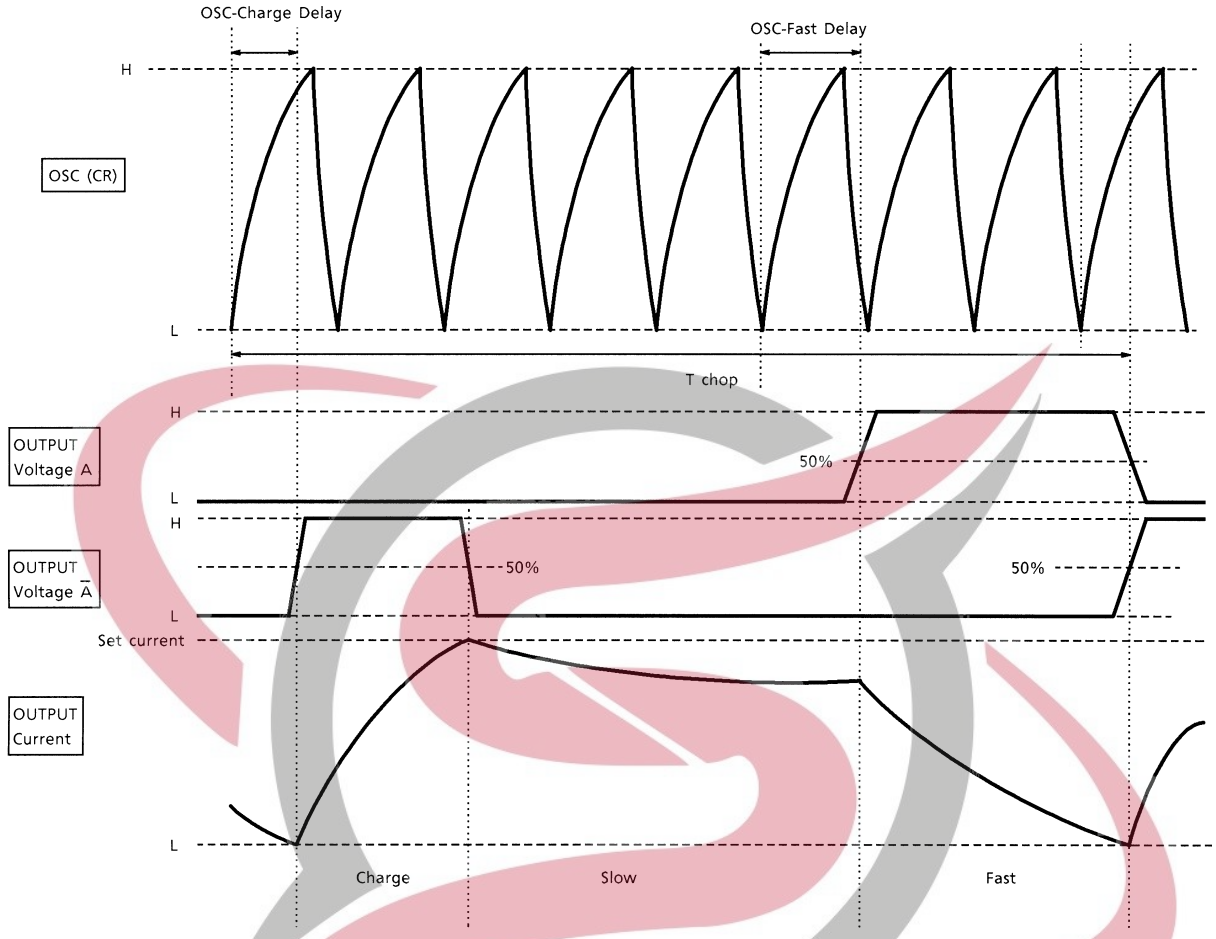
AC Characteristics (Ta = 25°C, V_M = 24 V, V_{DD} = 5 V, 6.8 mH/5.7 Ω)

Characteristics	SymboL	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock frequency	f_{CLK}	16	—	1.0	—	25	MHz
Minimum clock pulse width	$t_{w\ (CLK)}$	16	—	40	—	—	ns
	$t_{wp\ (CLK)}$			20	—	—	
	$t_{wn\ (CLK)}$			20	—	—	
Minimum STROBE pulse width	t_{STROBE}	16	—	40	—	—	ns
	$t_{STROBE\ (H)}$			20	—	—	
	$t_{STROBE\ (L)}$			20	—	—	
Data setup time	$t_{suSIN-CLK}$	16	—	20	—	—	ns
	$t_{suST-CLK}$			20	—	—	
Data hold time	$t_{hSIN-CLK}$	16	—	20	—	—	ns
	$t_{hCLK-ST}$			20	—	—	
Output transistor switching characteristic	t_r	18	Output Load ; 6.8 mH/5.7 Ω	—	0.1	—	μs
	t_f			—	0.1	—	
	$t_{pLH\ (ST)}$		STROBE (↑) to VOUT Output Load; 6.8 mH/5.7 Ω	—	15	—	
	$t_{pHL\ (ST)}$			—	10	—	
	$t_{pLH\ (CR)}$		CR to VOUT Output Load; 6.8 mH/5.7 Ω	—	1.2	—	
	$t_{pHL\ (CR)}$			—	2.5	—	
Noise rejection dead band time	t_{BLNK}	19	I_{out} = 1.0 A	200	300	400	ns
CR reference signal oscillation frequency	f_{CR}	20	C_{osc} = 560 pF, R_{osc} = 3.6 kΩ	—	800	—	kHz
Chopping frequency range	$f_{chop\ (min)}$ $f_{chop\ (typ.)}$ $f_{chop\ (max)}$	20	Output active (I_{out} = 1.0 A) Step fixed, Ccp1 = 0.22 μF, Ccp2 = 0.01μF	40	100	150	kHz
Chopping frequency	f_{chop}		Output active (I_{out} = 1.0 A) CR CLK = 800 kHz	—	100	—	kHz
Charge pump rise time	t_{ONG}	21	Ccp2 = 0.22μF, Ccp = 0.01 μF V_M = 24 V, V_{DD} = 5 V, $\overline{RESET}$ = L → H	—	2	4	ms

Test Waveforms (Timing waveforms and names)



Test Waveforms (Timing waveforms and names)



Calculation of Set Current

Determining R_{RS} and V_{ref} determines the set current value.

$$I_{out}\,(Max) = \frac{1}{V_{ref}\,(GAIN)} \times V_{ref}\,(V) \times \frac{T_{orque}\,(T_{orque} = 100, 85, 70, 50\%: \text{input serial data})}{R_{RS}\,(\Omega)}$$

1/5.0 is V_{ref} (gain) : V_{ref} attenuation ratio (typ.).

For example,

to input V_{ref} = 3 V and Torque = 100% and to output I_{out} = 0.8 A,
R_{RS} = 0.75 Ω (0.5 W or more) is required.

Formulas for Calculating CR Oscillation Frequency (Chopping reference frequency)

The CR oscillation frequency and f_{chop} can be calculated by the following formulas:

$$f_{CR} = \frac{1}{KA \times (C \times R \times KB \times C)}\ [Hz]$$

KA (constant): 0.523
KB (constant): 600

$$f_{chop} = \frac{f_{CR}}{8}\ [Hz]$$

Example : When Cosc = 1,000 pF and Rosc = 2.0 kΩ are connected, f_{CR} = 735 kHz.
At this time, the chopping frequency f_{chop} is : $f_{chop} = f_{CR}/8$ = 92 kHz.

Note: $f_{CR} = \frac{1}{t_{CR}}$

$$t_{CR} = t\,(Charge) + t\,(Dis\text{-}Charge)$$

CR oscillation cycle | CR charge time | CR distance time

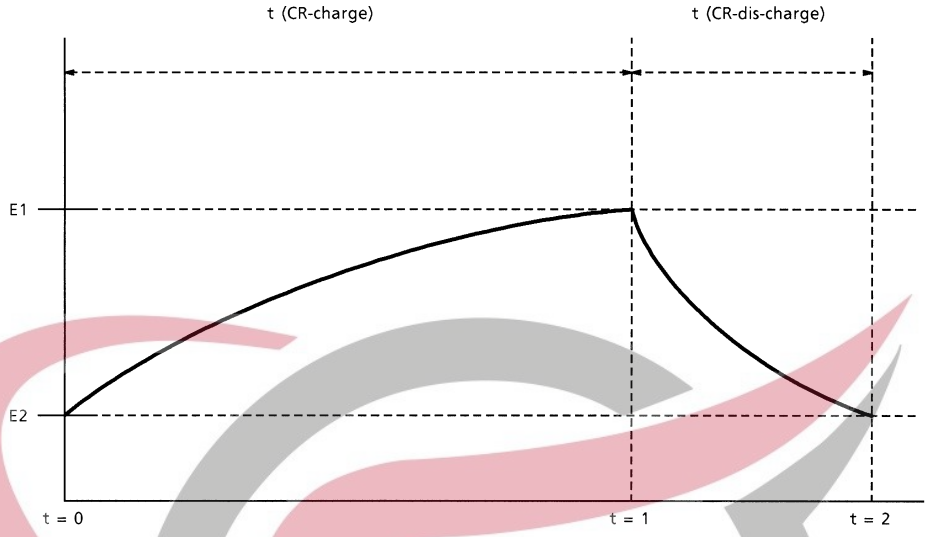
At this time, t (CR-discharge) is subject to the following condition:

600 ns > t (CR-discharge) > 400 ns.

Be sure to set the CR value in accordance with this condition.

CR Circuit Constants

OSC circuit oscillation waveform



The OSC circuit generates the chopping reference signal by charging and discharging the external capacitor Cosc through current supplied from the external resistor Rosc in the OSC block.
Voltages E1 and E2 in the diagram are set by dividing the V_{DD} by approximately 3/5 (E1) and 2/5 (E2).
The actual current chopping time is 1/8 the CR frequency.

[Important: Setting the CR Circuit Constants]

The CR oscillation waveform is converted in the IC to the CLK waveform (CR-CLK signal) and used for control.
If the CR waveform discharge time is set outside the range shown below, the operation of the IC is not guaranteed.
Be sure to set the CR waveform discharge time within the following range.

600 ns > t (CR discharge) > 400 ns

IC Power Dissipation

IC power dissipation is classified into two: power consumed by transistors in the output block and power consumed by the logic block and the charge pump circuit.

(1) Power consumed by the Power Transistor (calculated with R_{on} = 1.3 Ω)

In Charge mode, Fast Decay mode, or Slow Decay mode, power is consumed by the upper and lower transistors of the H bridges. The following expression expresses the power consumed by the transistors of a H bridge.

$$P\ (out) = 2\ (T_r) \times I_{out}\ (A) \times V_{DS}\ (V) = 2 \times I_{out}\text{^}2 \times R_{on} \quad \cdots\cdots (1)$$

The average power dissipation for output under 4-bit micro step operation (phase difference between phases A and B is 90°) is determined by expression (1).
Thus, power dissipation for output per unit is determined as follows (2) under the conditions below.

R_{on} = 1.3 Ω (@1.0 A)
I_{out} (Peak : Max) = 0.6 A
V_M = 24 V
V_{DD} = 5 V

$$P\ (out) = 2\ (T_r) \times 0.6\ (A)\text{^}2 \times 1.3\ (\Omega) \quad \cdots\cdots (2)$$
$$= 0.936\ (W)$$

(2) Power consumed by the logic block and IM

The following standard values are used as power dissipation of the logic block and IM at operation.

I (LOGIC) = 2 mA (Typ.): /unit
I (IM3) = 12.5 mA (Typ.): operation/unit
I (IM1) = 6.0 mA (Typ.): stop/unit

The logic block is connected to V_{DD} (5 V). IM (total of current consumed by the circuits connected to V_M and current consumed by output switching) is connected to V_M (24 V). Power dissipation is calculated as follows:

$$P\ (Logic\ and\ IM) = 5\ (V) \times 0.002\ (A) + 24\ (V) \times 0.0125\ (A) \quad \cdots\cdots (3)$$
$$= 0.31\ (W)$$

(3) Thus, power dissipation for 1 unit (P) is determined as follows by (2) and (3) above.

$$P = P\ (out) + P\ (Logic\ and\ IM) = 1.246\ (W)$$

Power dissipation for 1 unit at standby is determined as follows:

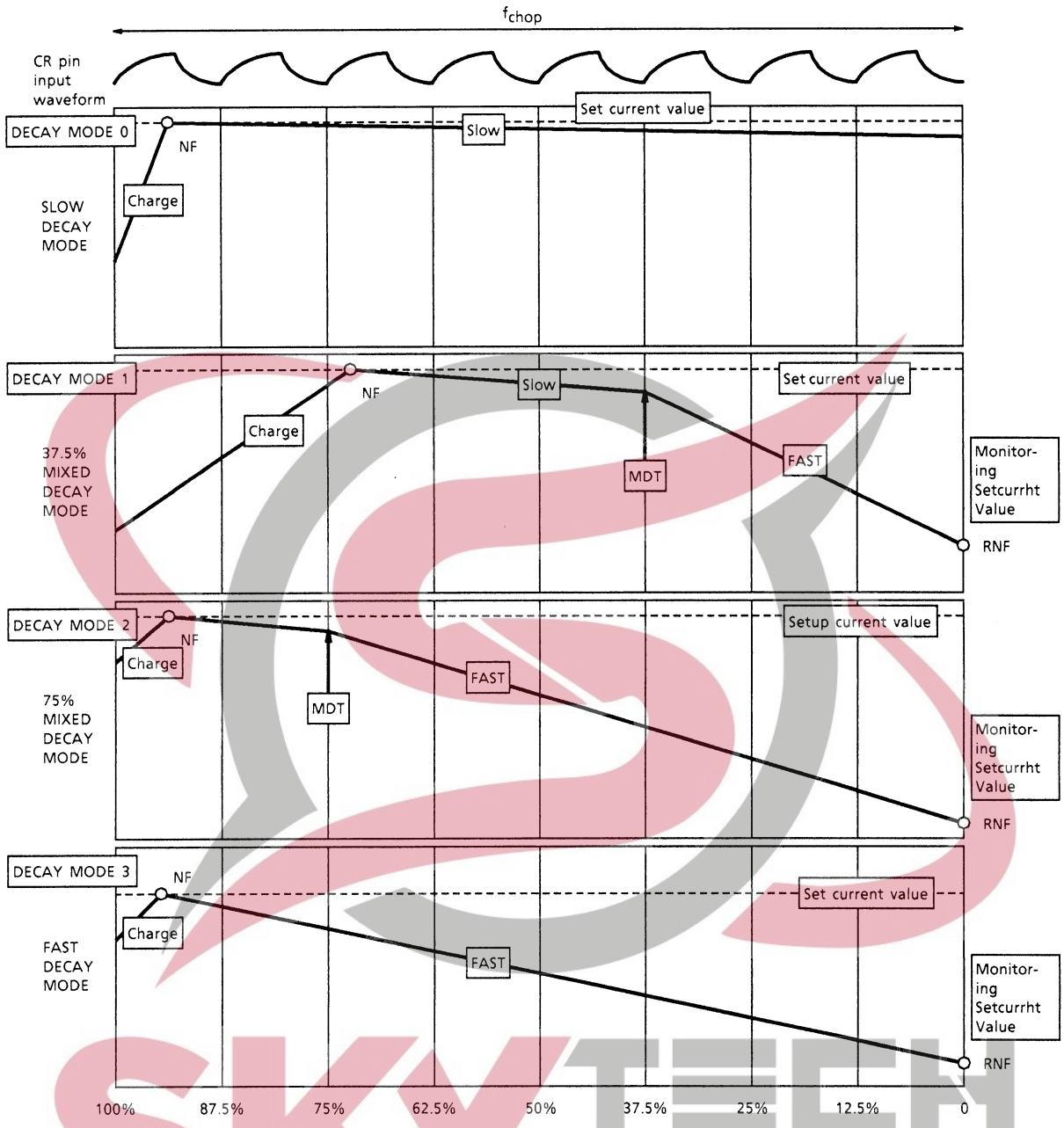
$$P\ (standby) = 24\ (V) \times 0.006\ (A) + 5\ (V) \times 0.002\ (A)$$
$$= 0.154\ (W)$$

When one motor driving = 100 %, power dissipation is determined as follows:

$$P\ (all) = 1.246\ (W) + 0.154\ (W) = 1.4\ (W)$$

For thermal design on the board, evaluate by mounting the IC.

MIXED DECAY Mode Waveforms (concept of mixed decay mode)

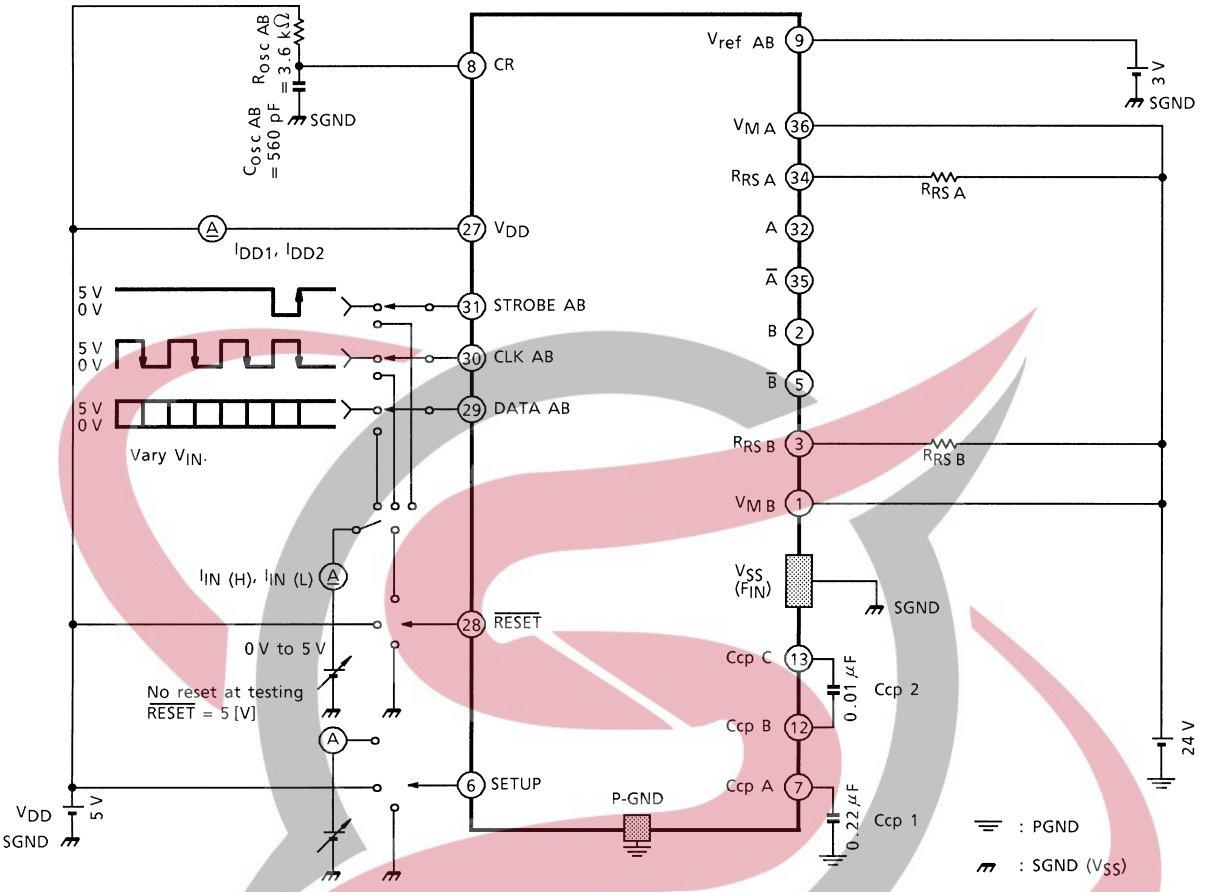


NF is the point where the output current reaches the set current value. RNF is the timing for monitoring the set current.

In Mixed Decay and Fast Decay modes, where the condition RNF (set current monitor signal) < (output current) applies, Charge mode is cancelled at the next chopping cycle (charge cancel circuit). Therefore, at the next chopping cycle, the IC enters Slow + Fast modes (Slow → Fast at MDT).

Test Circuit (A/B unit only. C/D unit conforms to A/B unit.)

1. $V_{IN\ (H)}$, $V_{IN\ (L)}$

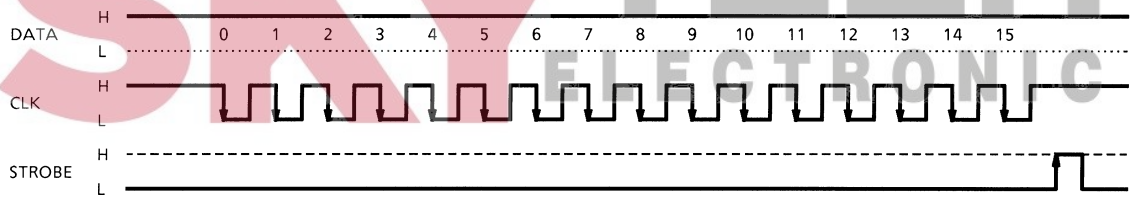


Test method

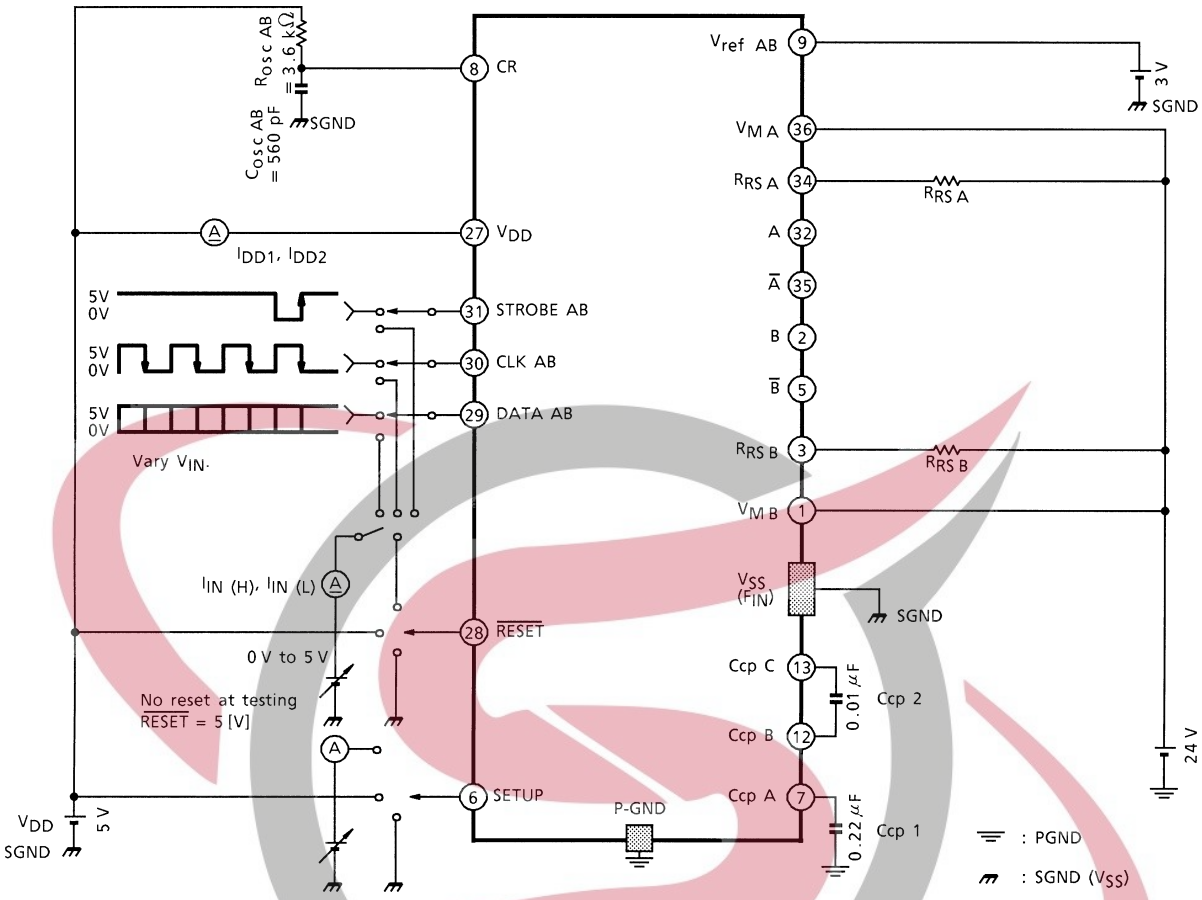
V_{IN} (H): Set $\overline{RESET}$ to High and vary the logic input voltage from 0 to 7 V.
Monitor I_{DD} and measure the change point (V_M = 24 V).

V_{IN} (L): Set $\overline{RESET}$ to High and vary the logic input voltage from 5 to 0 V.
Monitor I_{DD} and measure the change point.

Setup data



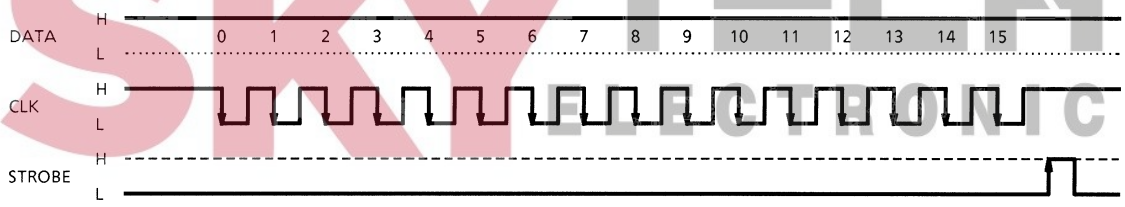
2. $I_{IN\ (H)}$, $I_{IN\ (L)}$, I_{DD1}, I_{DD2} (A/B unit only. C/D unit conforms to A/B unit.)



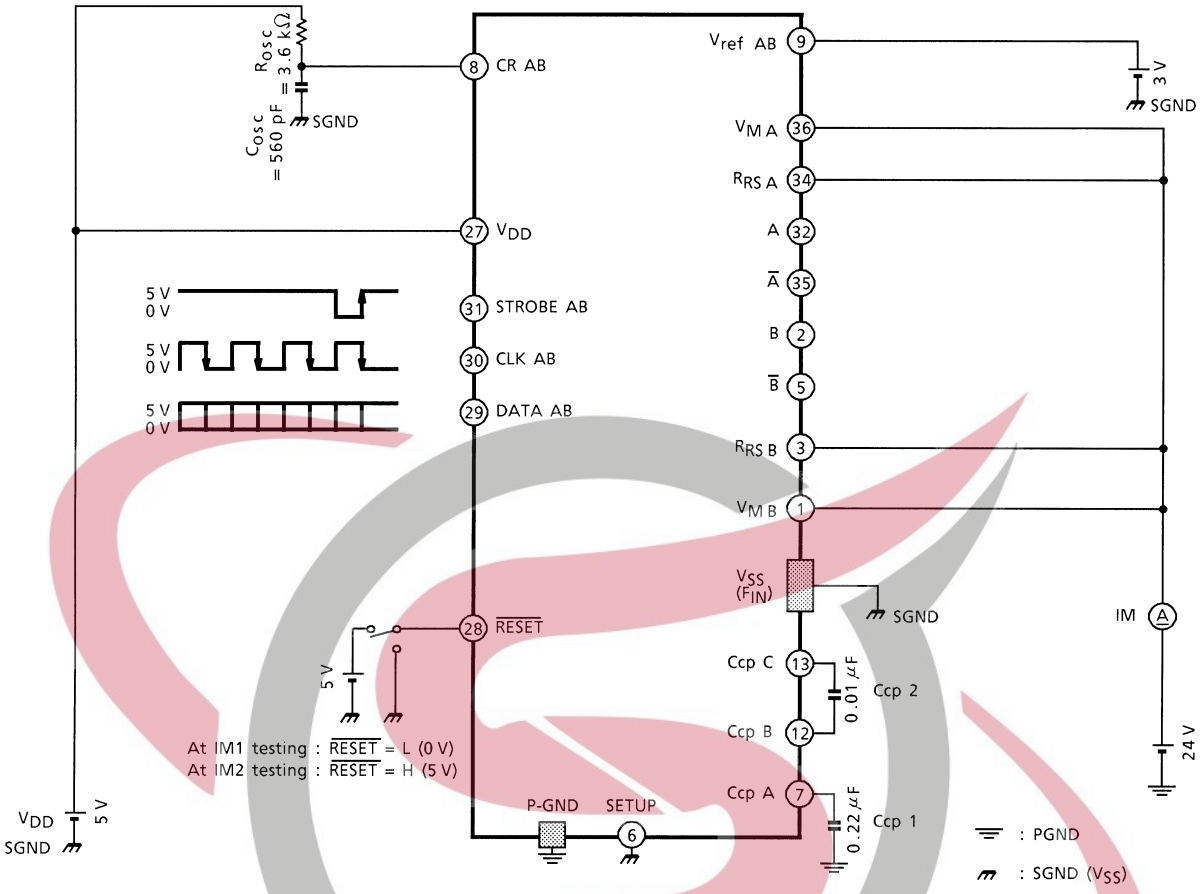
Test method

$I_{IN\ (H)}$: Set $\overline{RESET}$ to High, set the the logic input voltage to 5 V, and measure the input current.
$I_{IN\ (H)}$: Set $\overline{RESET}$ to High, set the the logic input voltage to 0 V, and measure the input current.
I_{DD1}: Apply V_{DD}, input RESET, and measure I_{DD}.
I_{DD2}: Input 6.25 MHz clock and measure the current when the logic is operating. Set output to OPEN.

Setup data



3. IM_1, IM_2 (A/B unit only. C/D unit conforms to A/B unit.)

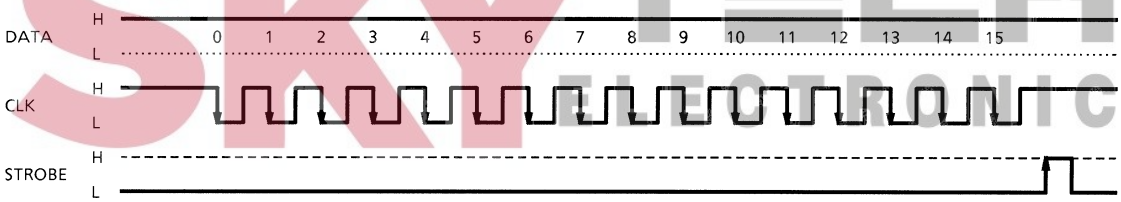


Test method

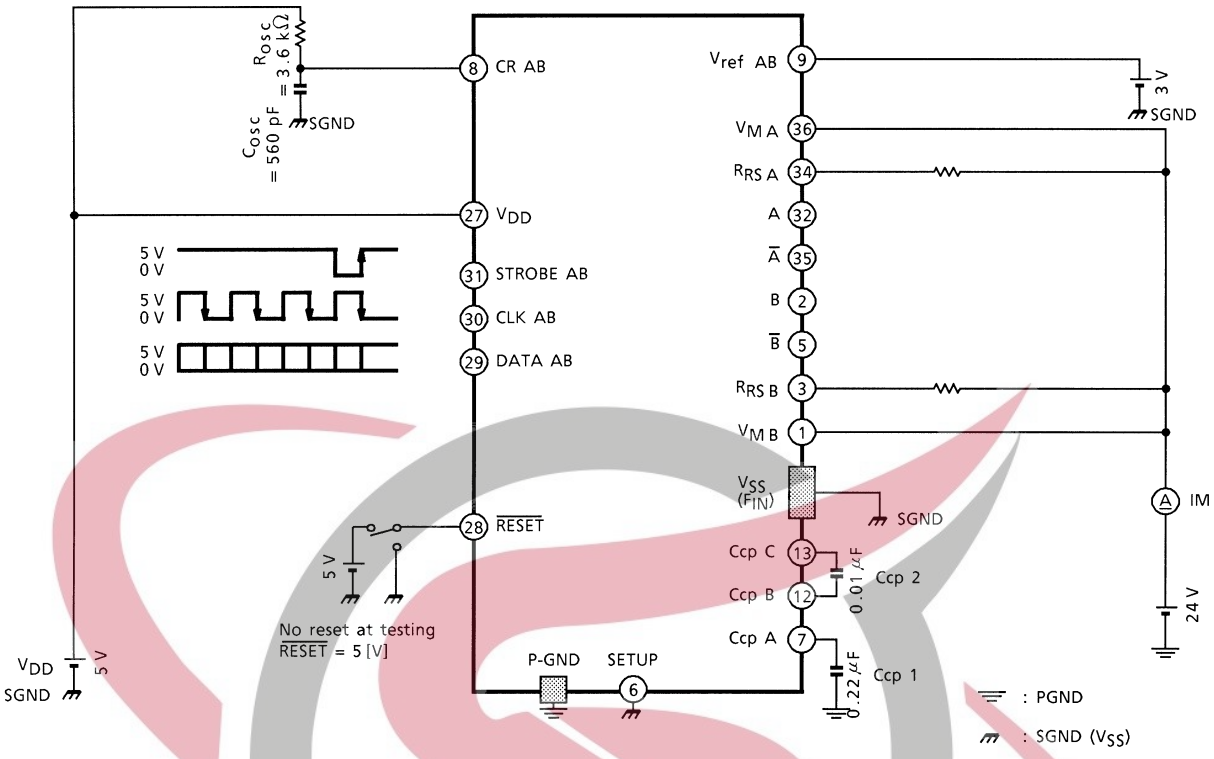
IM_1: Set the logic block to non-active (DATA = all 0), V_{DD} = 5 V, V_M = 24 V, and output to open. Measure the current input from V_M supply. $\overline{RESET}$ = L

IM_2: Set the logic block only to active (CLK = 6.25 MHz), V_M = 24 V, and output to open. Measure the current input from V_M supply. $\overline{RESET}$ = H

Setup data



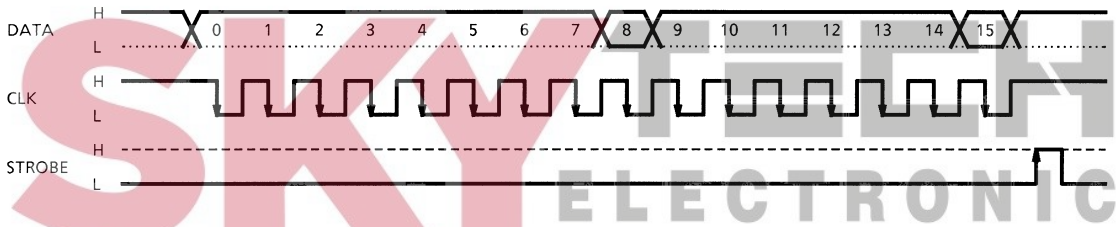
4. IM_3 (A/B unit only. C/D unit conforms to A/B unit.)



This is the IM current when all of the circuits, including the output transistors, in the IC are operating.
The IM current includes the current dissipation in the charge pump circuit, output gate loss, and output predriver.
Because the IM current (IM_3) is input from the RS pin, which is also used for the output current, IM_3 cannot be measured by the normal testing methods.
Use the method shown below.

Setup data

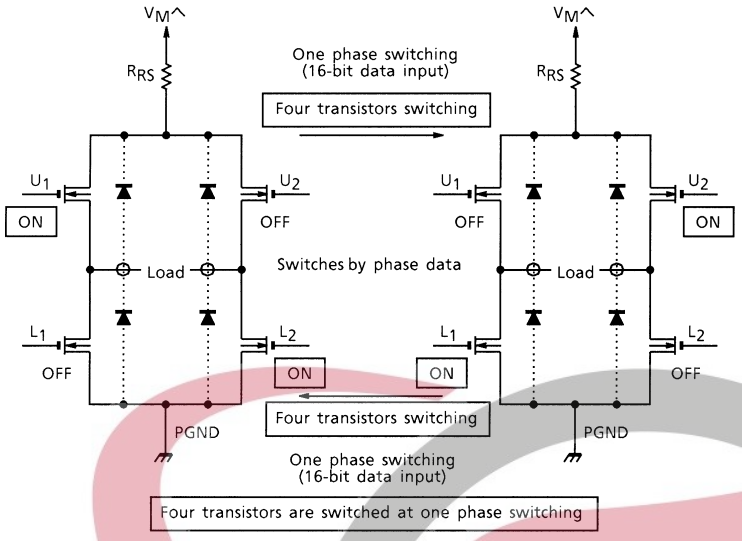
The serial data PHASE signal (both A and B) switch over to high or low.



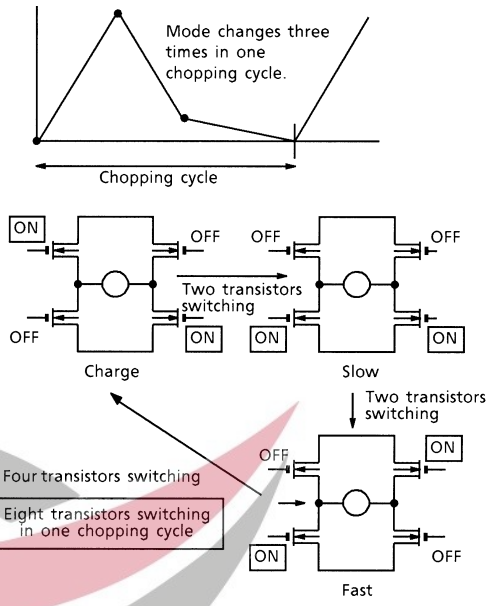
Test method

Set output to open, change phase data from 1 → 0 → 1 → 0 and perform switching. When testing, input phase data at double the chopping frequency (if f_{chop} = 100 kHz, fDATA = 200 kHz) and measure the current value of V_M supply.
fDATA = 200 kHz means that the phase switches at 200 kHz.

Number of switchings at phase switching

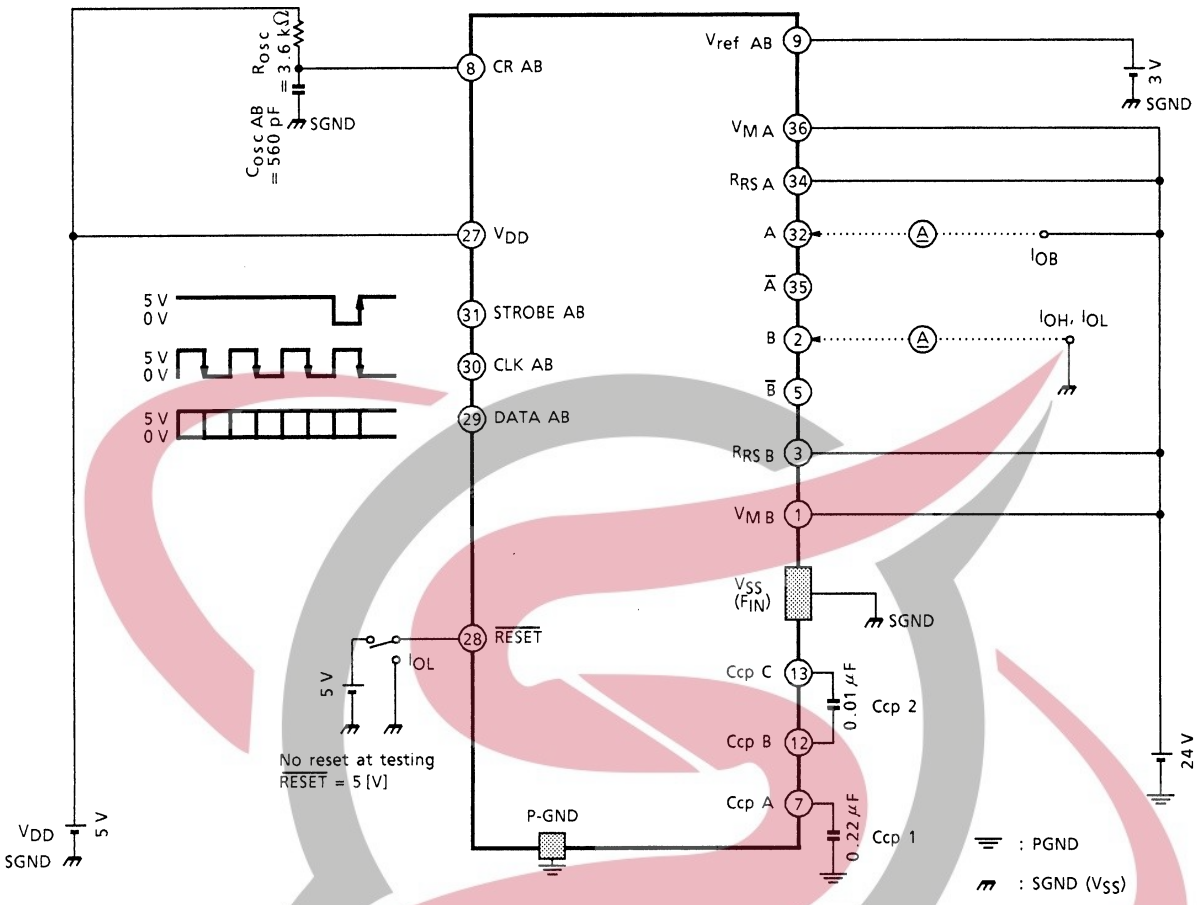


Number of switchings at actual operation



Number of switchings at actual operation = 2 × number of switchings at phase switching.
Therefore, switching the phase at 2 × chopping cycle matches the number of switchings at actual operation with the number of switchings at phase switching, and allows the actual current dissipation, IM_3, to be measured.

5. I_{OB}, I_{OH}, I_{OL} (A/B unit only. C/D unit conforms to A/B unit.)



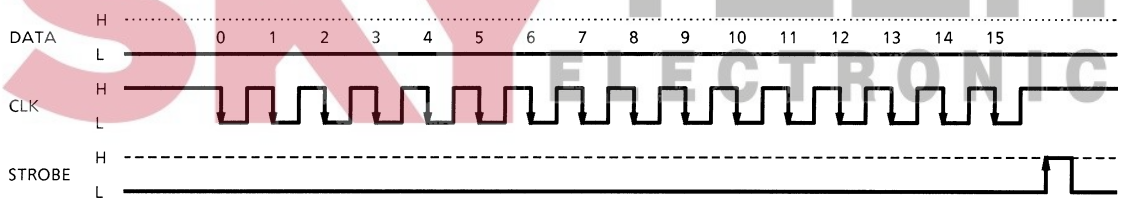
Test method

I_{OH}: With V_M = 24 V, V_{DD} = 5 V, and logic input all = 0 applied, set $\overline{RESET}$ = H, connect the output pins to GND, and measure the supply current.

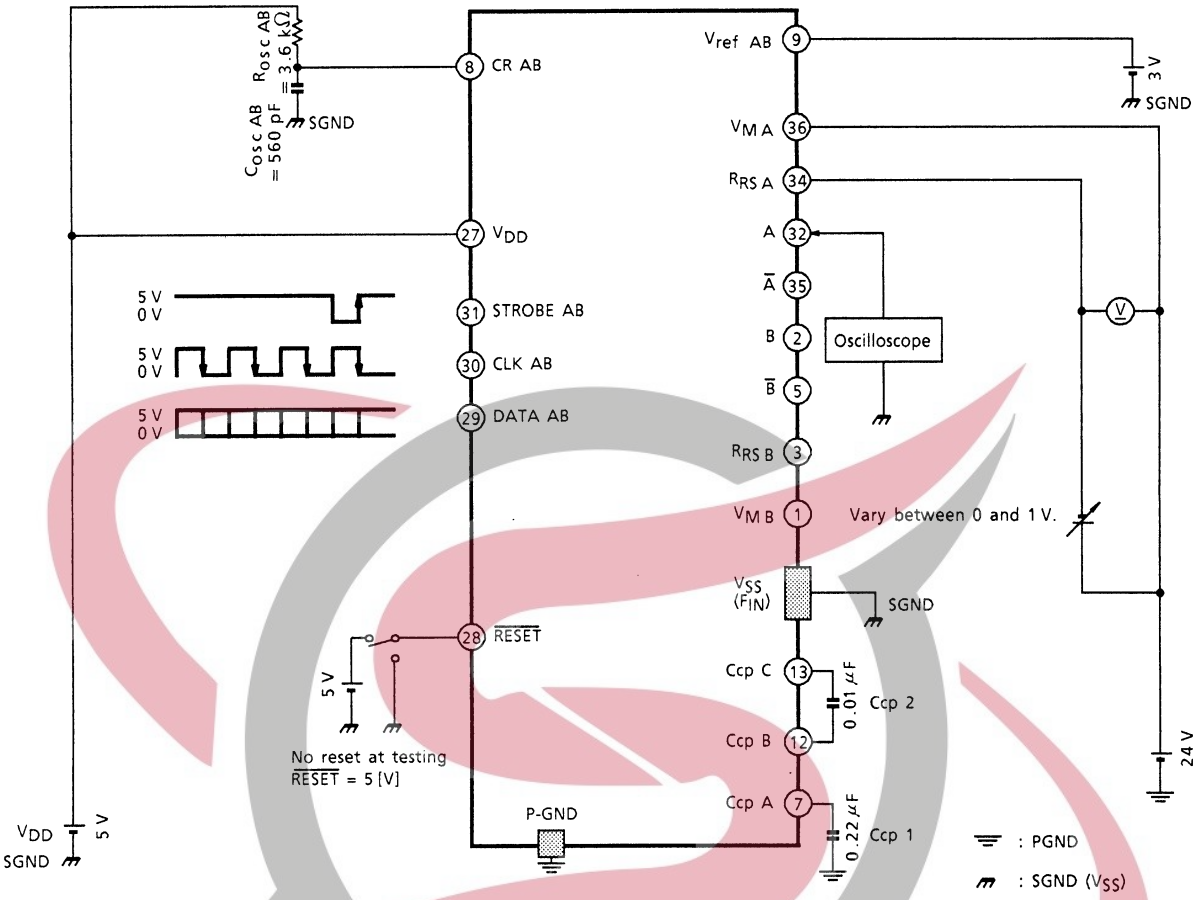
I_{OB}: With V_M = 24 V, V_{DD} = 5 V, and logic input all = 0 applied, set $\overline{RESET}$ = H, connect the output pins to V_M, and measure the supply current.

I_{OL}: With V_M = 24 V, V_{DD} = 5 V, and logic input all = 0 applied, set $\overline{RESET}$ = L, connect the output pins to GND, and measure the supply current.

Setup data



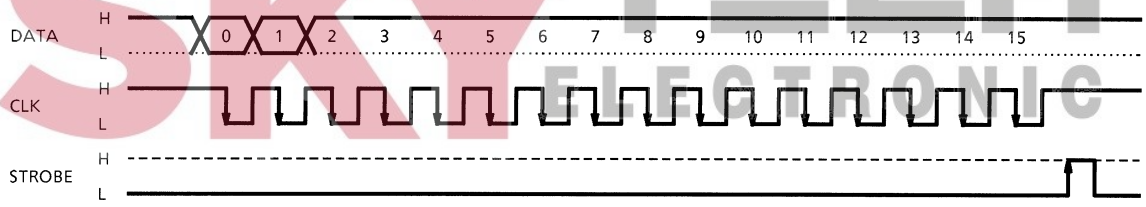
6. V_{RS} (H to L), V_{ref} (GAIN) (when measuring phase A) after measurement
(A/B unit only. C/D unit conforms to A/B unit.)



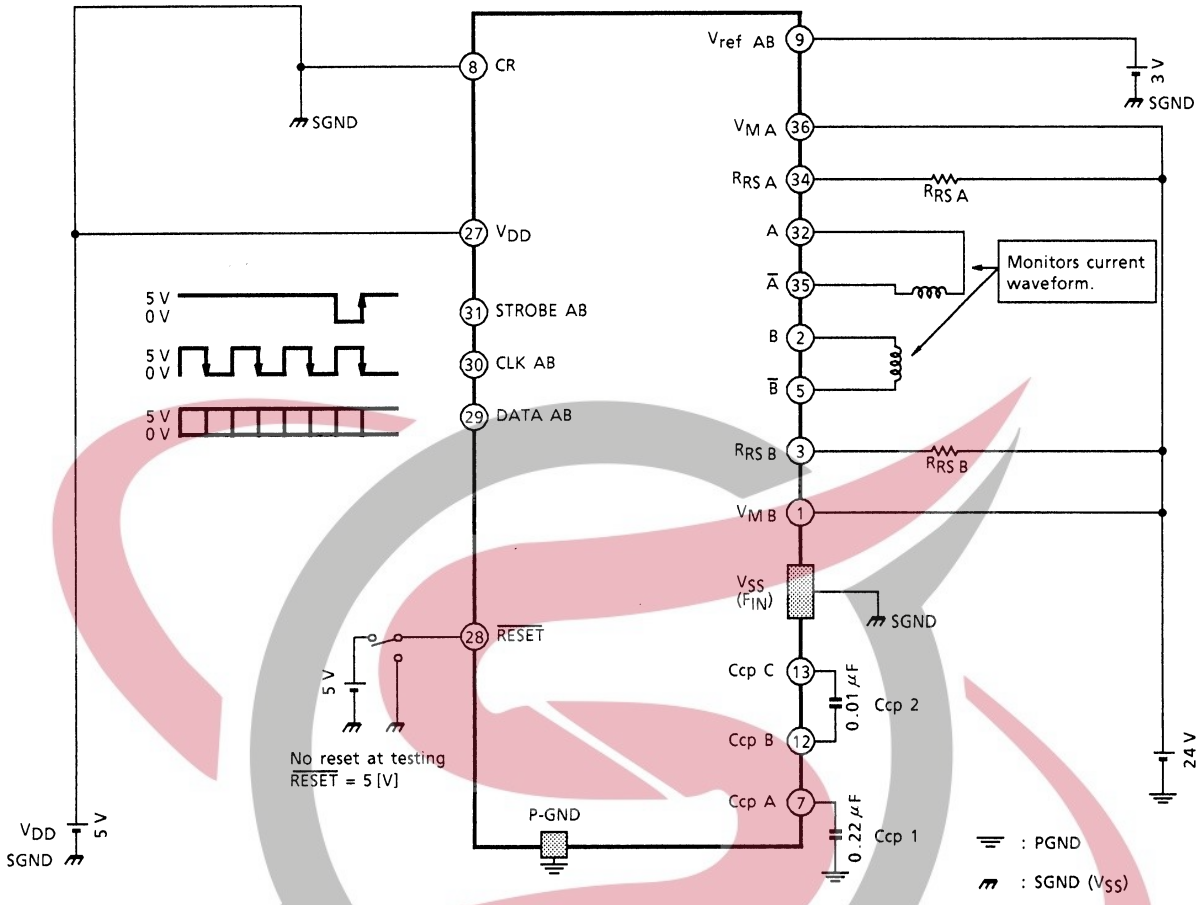
V_{RS} (H to L): Input torque data = 100% (HH) and vary the voltage between V_M and R_S pins.
Measure the voltage (V_{RS}) when output changes from fixed Charge mode to another mode.
Also measure V_{RS} when torque data = 85% (HL), 70% (LH), or 50% (LL) as above and calculate the ratio using V_{RS} value at 100% as reference.

V_{ref} (GAIN): $V_{ref\ (GAIN)} = \dfrac{V_{RS}\ (*)}{V_{ref}}$ ((*) V_{RS}: when torque data = 100%)

Setup data

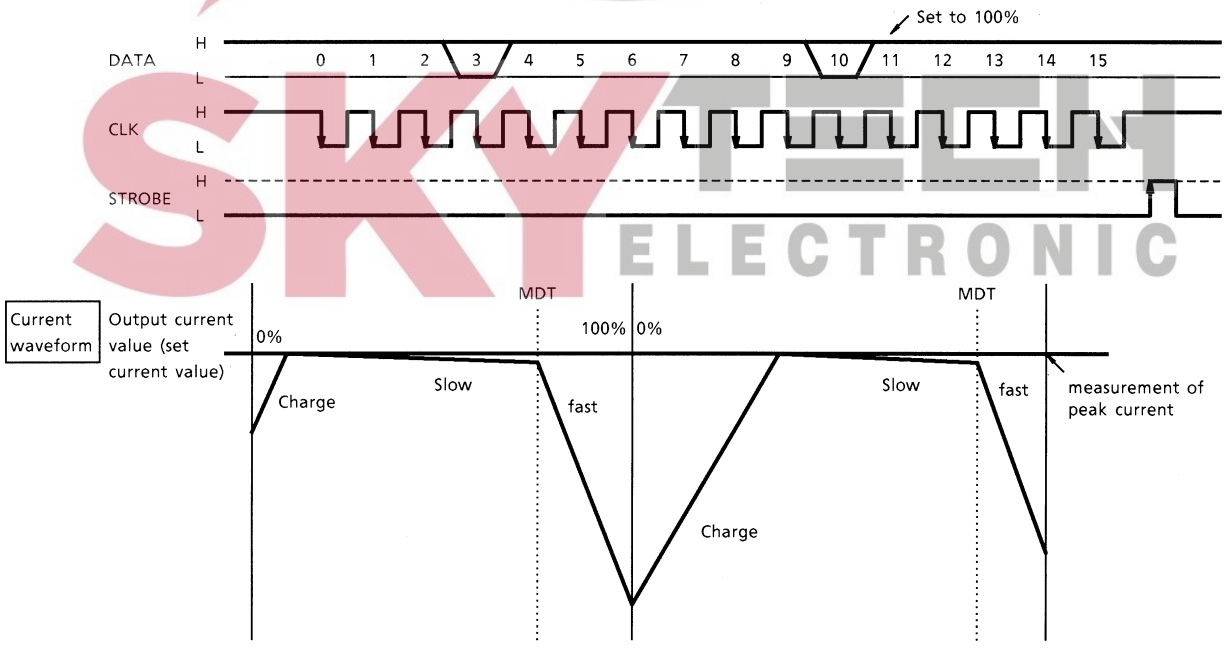


7. ΔI_{out1}, ΔI_{out2} (A/B unit only. C/D unit conforms to A/B unit.)

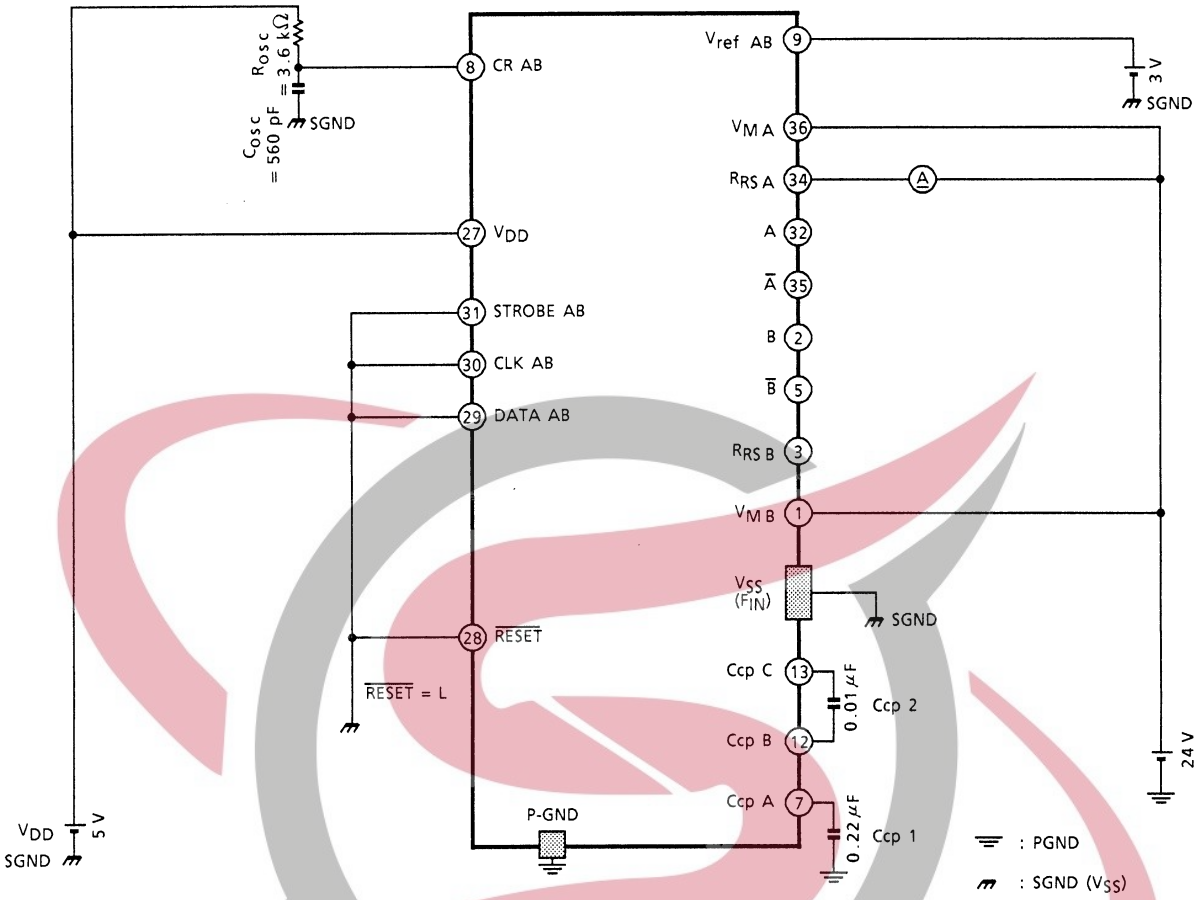


With L load, perform chopping in Mixed Decay mode. Monitor the output current waveform and measure the various output currents at constant current operation.

Setup data

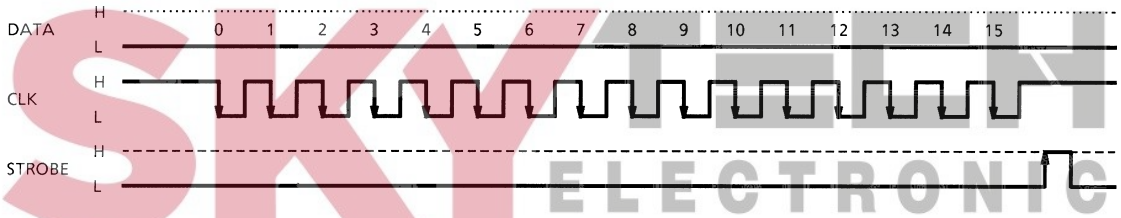


8. I_{RS} (when measuring phase A) (A/B unit only. C/D unit conforms to A/B unit)

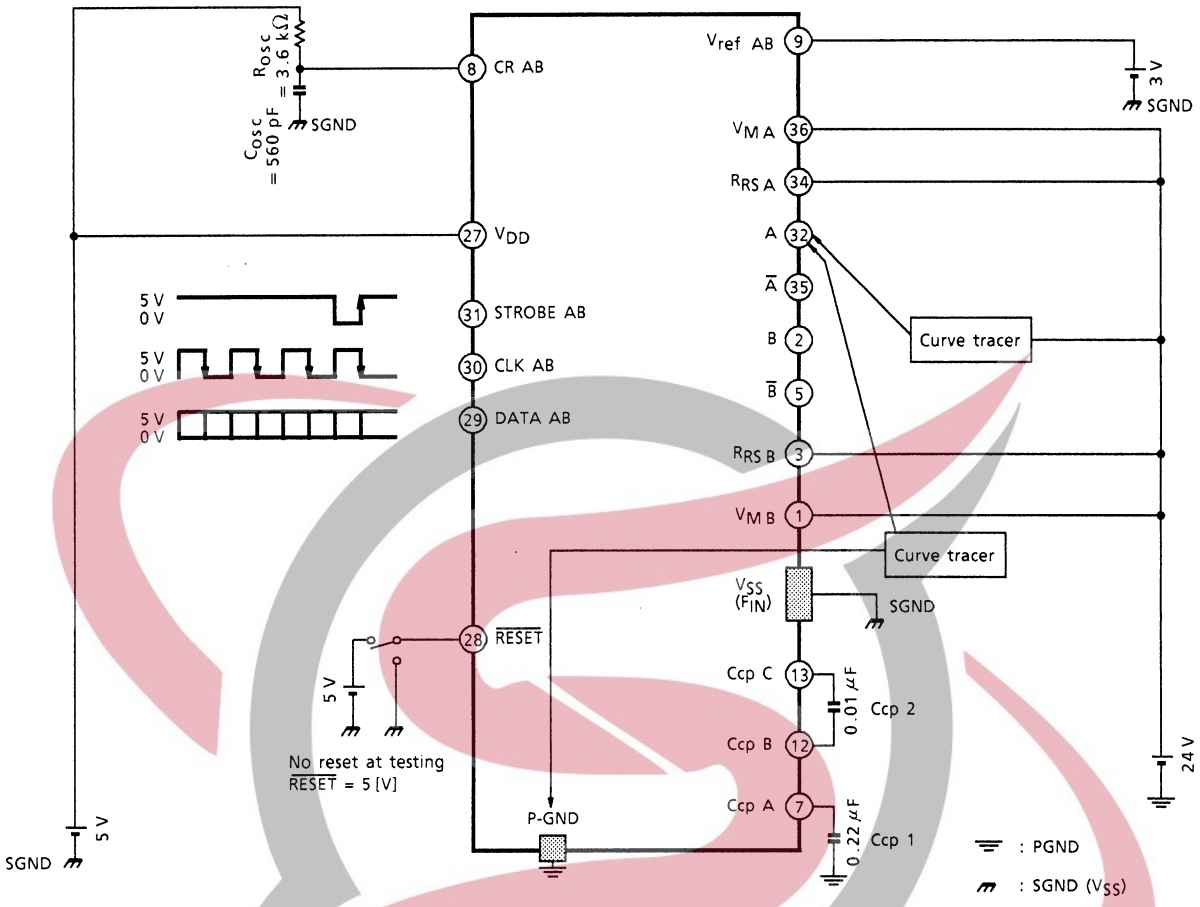


With L input to $\overline{\text{RESET}}$, connect V_M and R_{RS} to the power supply, and measure the current input to the RS pin. (Either drop all the input pins to GND level or input all Low data to the DATA pin, then perform measurement. At that time, leave all other output pins open.)

Setup data

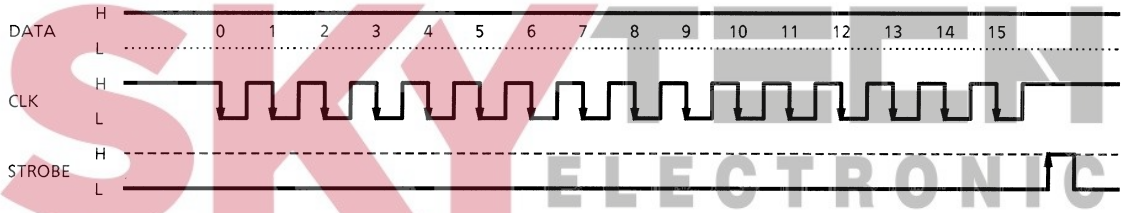


9. $R_{ON\ (D-S)}$, $R_{ON\ (S-D)}$ when measuring output A (A/B unit only. C/D unit conforms to A/B unit.)

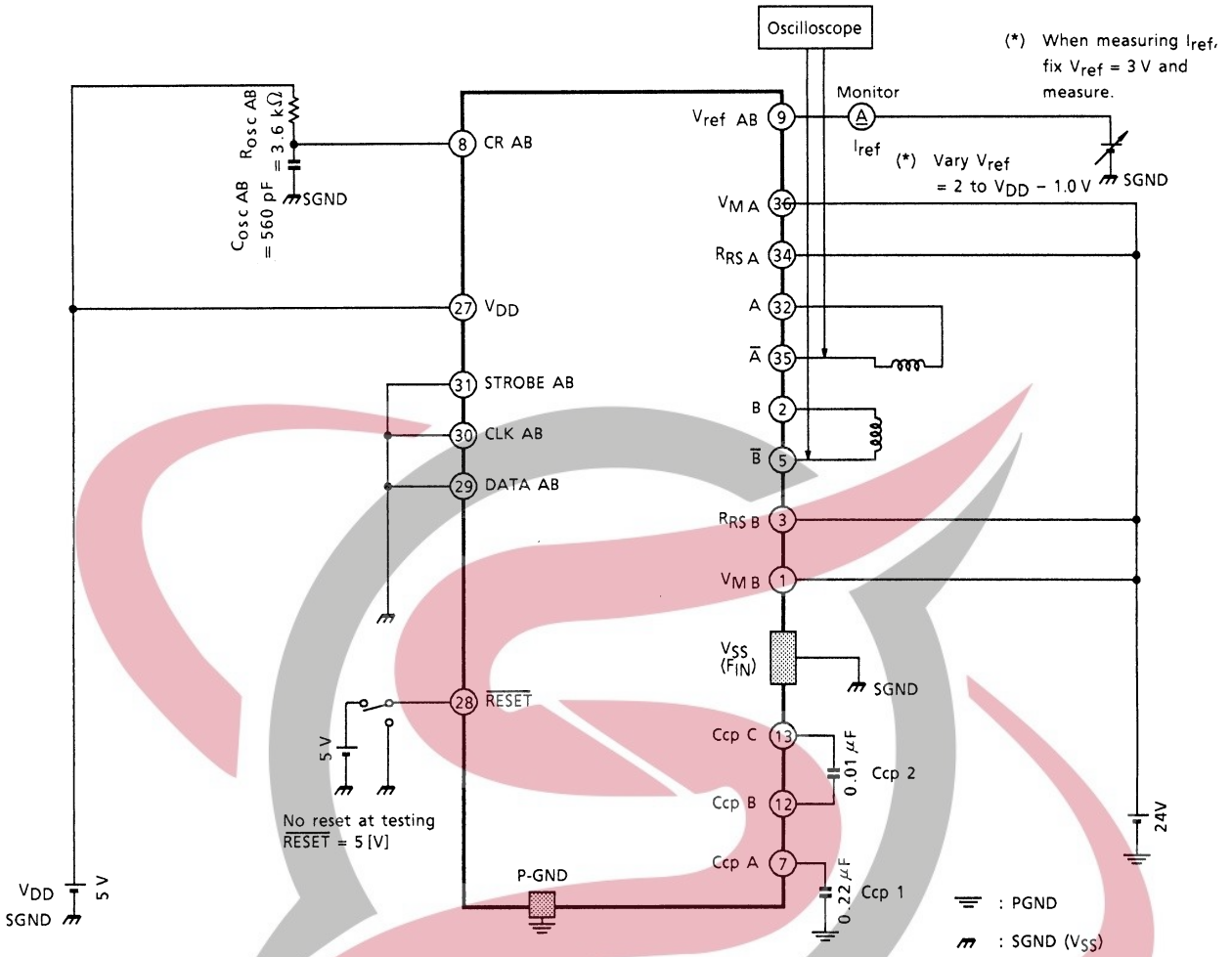


Input the current setting data (HHHH signal) to the DATA pin and measure the voltage between V_M and OUT when I_{out} = 1000 mA or the voltage between OUT and GND. Then, change the phase and repeat measurement. At that time, leave the output pins which are not measured open.

Setup data (Vary the phase data during testing.)



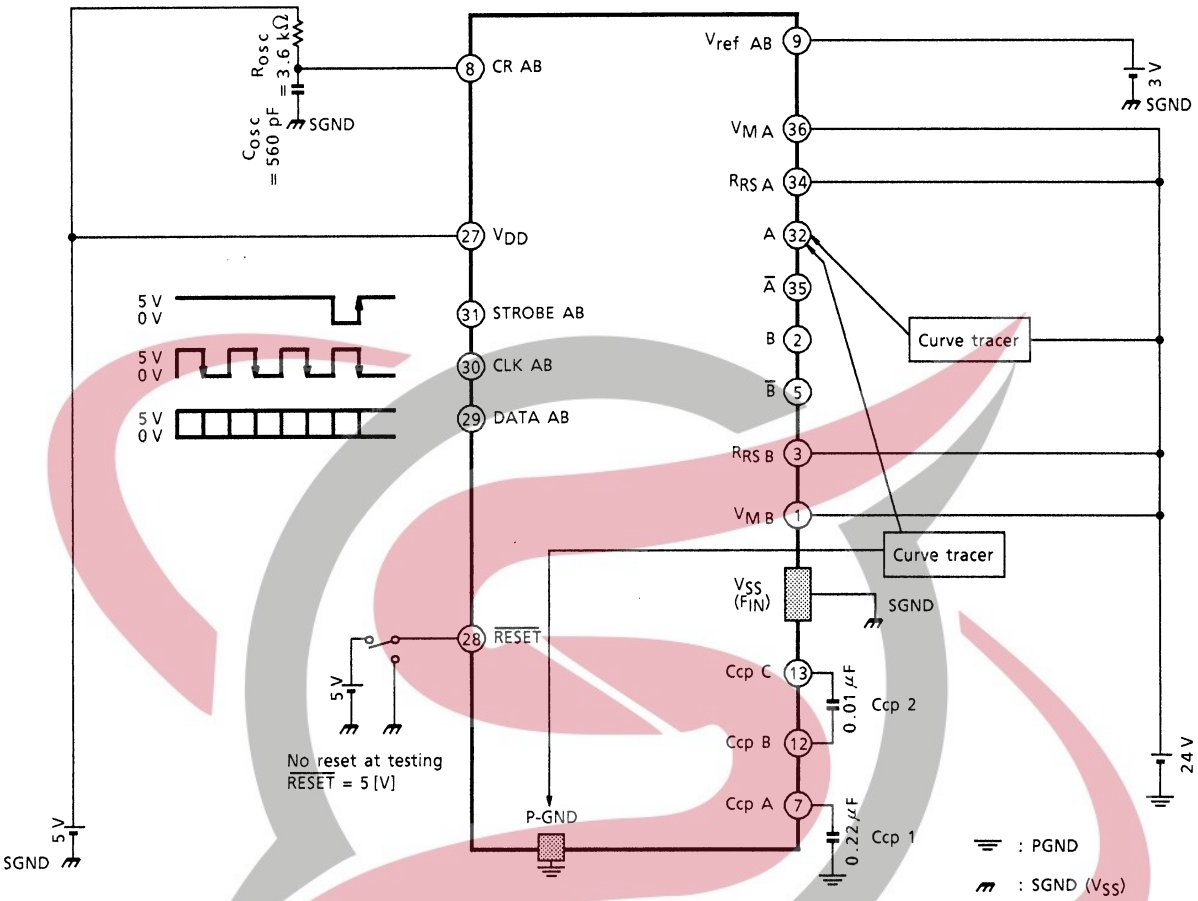
10. V_{ref}, I_{ref} (A/B unit only. C/D unit conforms to A/B unit.)



V_{ref}: Vary V_{ref} = 2 to V_{DD} − 1 V and confirm that output is on.

I_{ref}: When V_M = 24 V and V_{DD} = 5 V, apply the specified voltage of 3 V to the V_{ref} and monitor the current flow value.

11. T_jTSD, ΔT_jTSD (Measure in an environment such as an constant temperature chamber where the temperature for the IC can be freely changed) (A/B unit only. C/D unit conforms to A/B unit.)

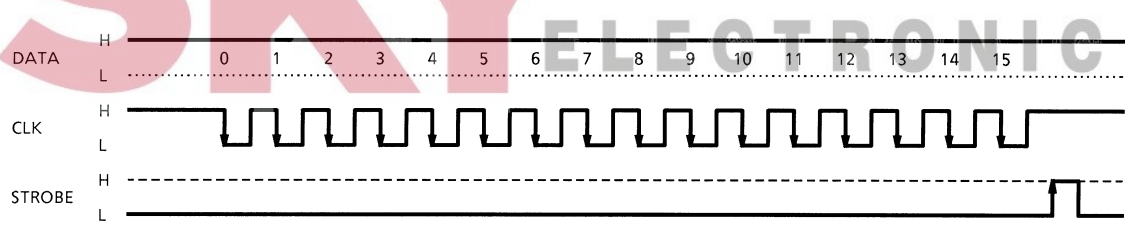


T_jTSD: Increase the ambient temperature. Measure the temperature when output stops.

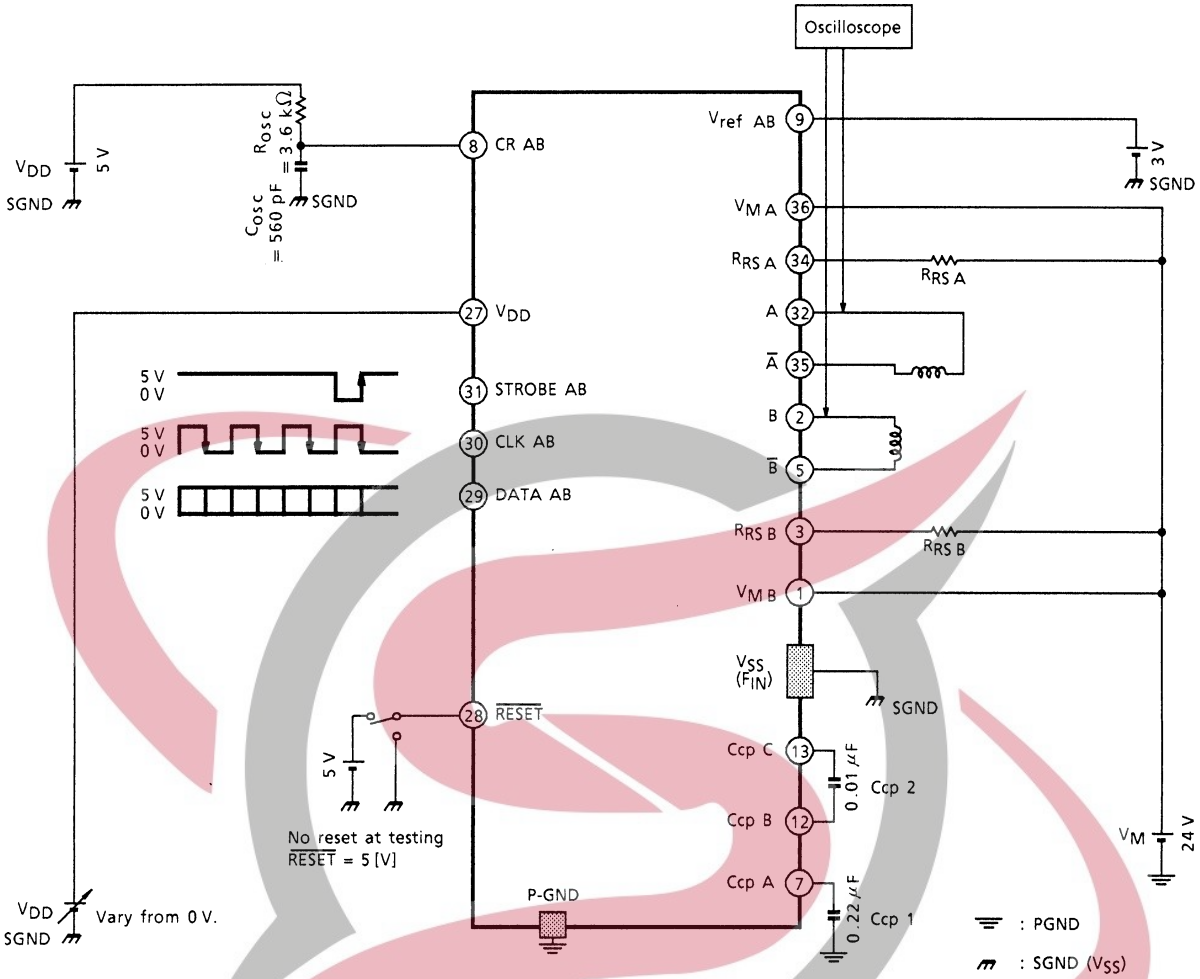
ΔT_jTSD: Gradually lower the temperature from the level when the TSD circuit was operating (output off). At that time, control the RESET input thus : H → L → H → L. Output will begin at a certain temperature level.

ΔT_jTSD is the difference between the temperature at which output begins and the temperature at which TSD is triggered.

Setup data

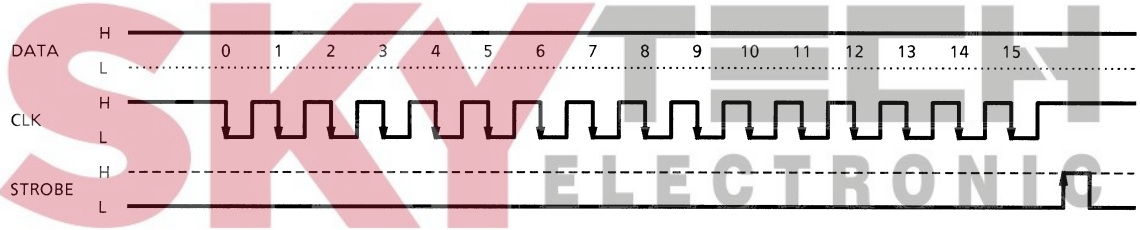


12. V_{DDR} (A/B unit only. C/D unit conforms to A/B unit.)

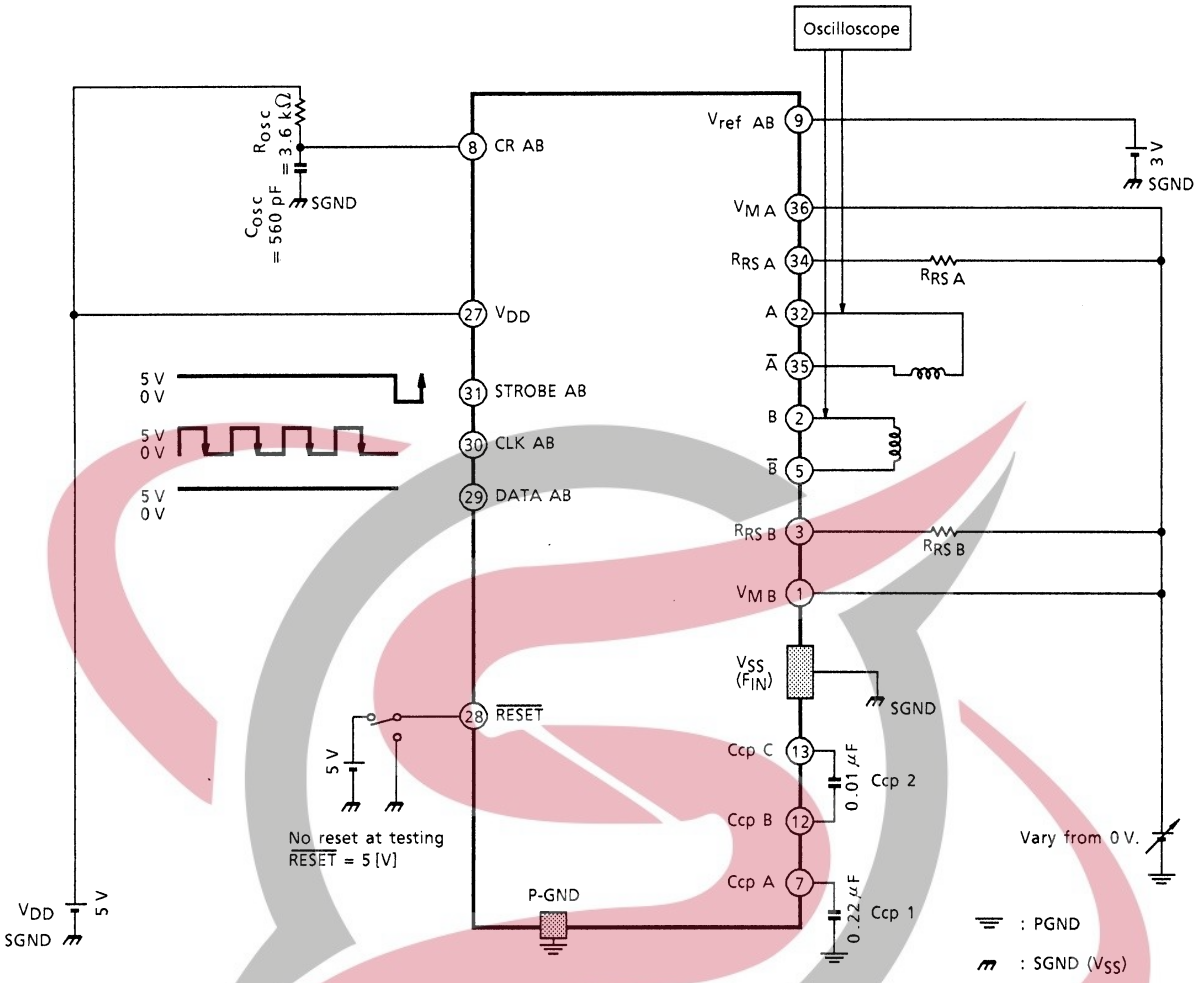


Monitor the output pins. Increase the V_{DD} voltage from 0. Measure the V_{DD} value when output starts. Next, decrease the V_{DD} voltage and measure the V_{DD} value when output stops.

Setup data

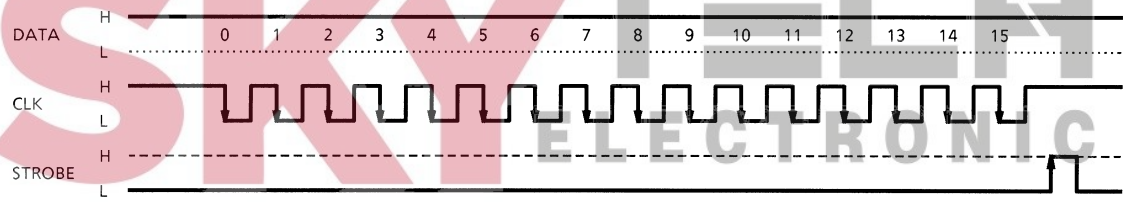


13. V_{MR} (A/B unit only. C/D unit conforms to A/B unit.)

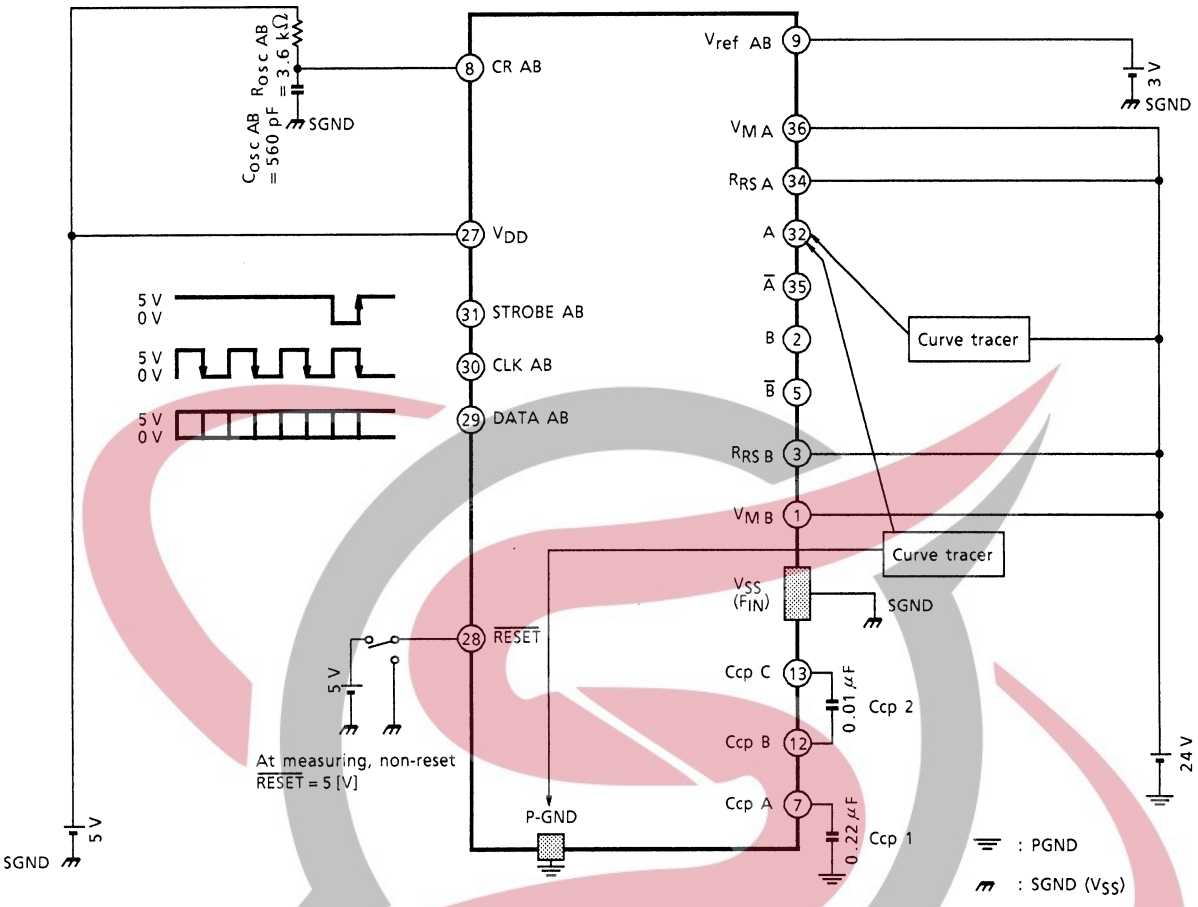


With the CLK signal and DATA (all High) input, increase the V_M voltage from 0.
Measure the V_M value when output starts.
Next, decrease the V_M voltage and measure the V_M value when output stops.

Setup data



14. Overcurrent protector circuit (ISD) (To measure output A :)
(A/B unit only. C/D unit conforms to A/B unit.)



Test method: To monitor operating current of the overcurrent protector circuit when output A is short-circuited to the power supply

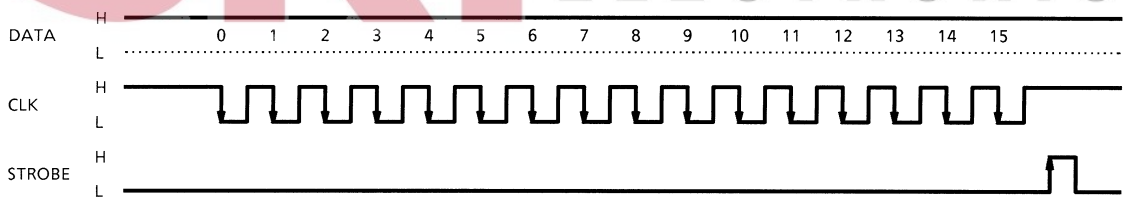
Input the current setting data (HHHH signal) to the DATA pin. If short-circuited to the supply, measure the lower output transistors. If short-circuited to ground, measure the upper output transistors (see how to measure R_{ON}).

When measuring R_{ON}, increase the current flow. There is a current value at which output is switched off and R_{ON} cannot be measured. This value is the set current value for the overcurrent protector circuit.

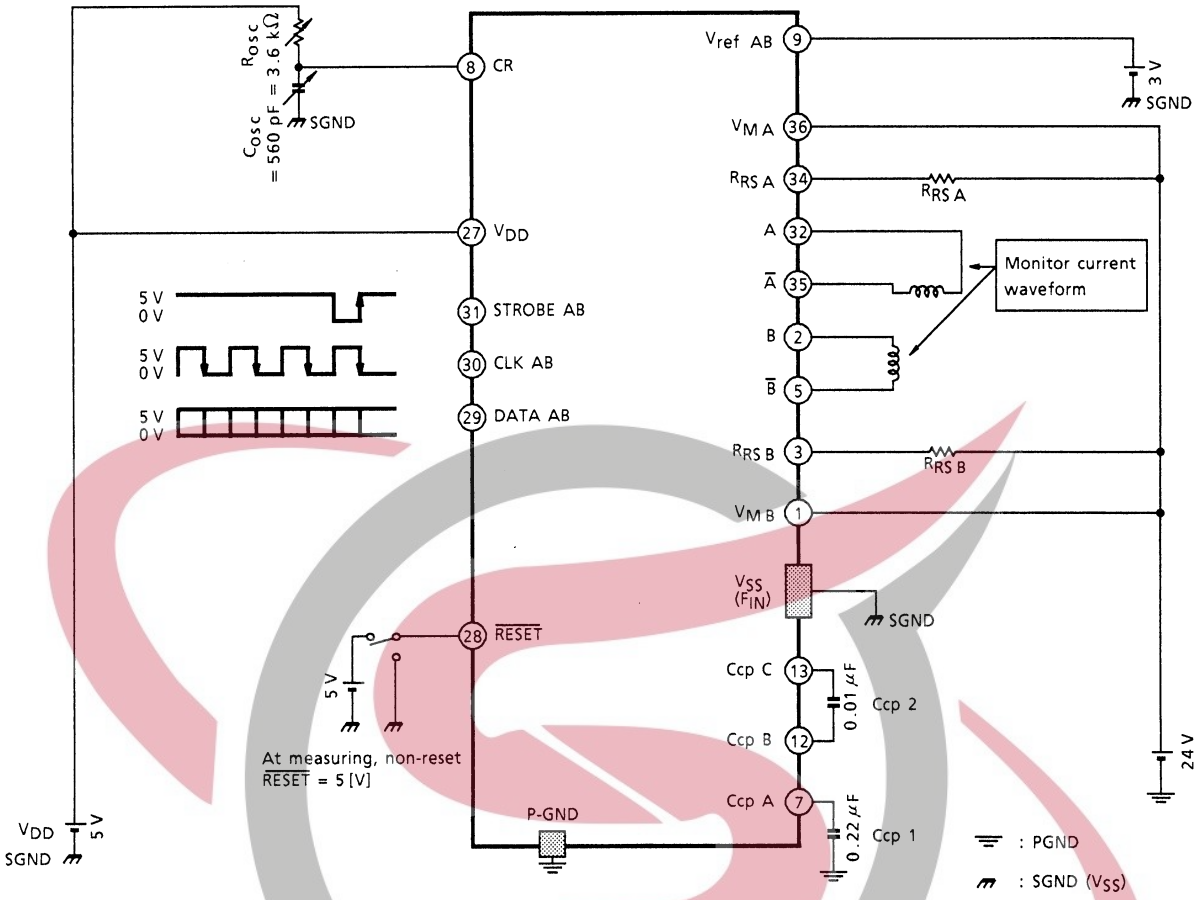
Make sure to leave open the output pins not being measured.

Note that if the temperature changes, the value may fluctuate. Try to avoid applying power to the IC by one-shot measuring.

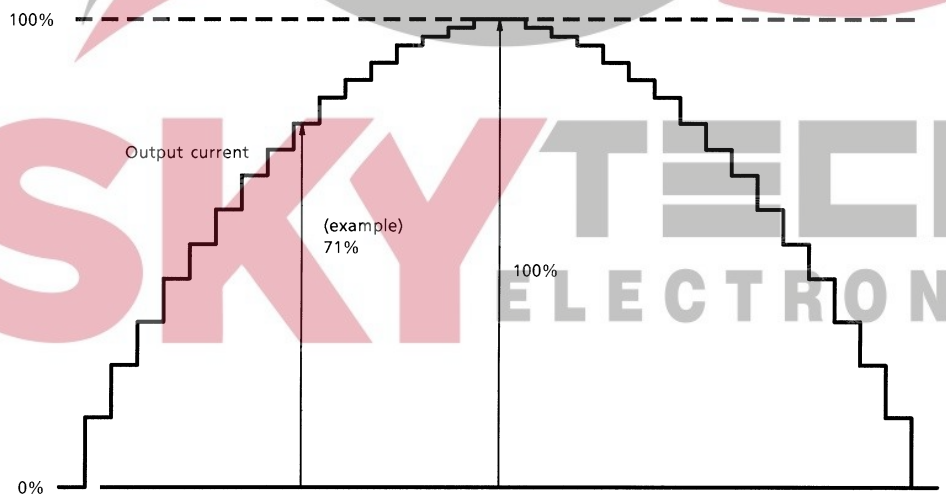
Setup data (Example : The phase signal must be changed depending on the pin.)



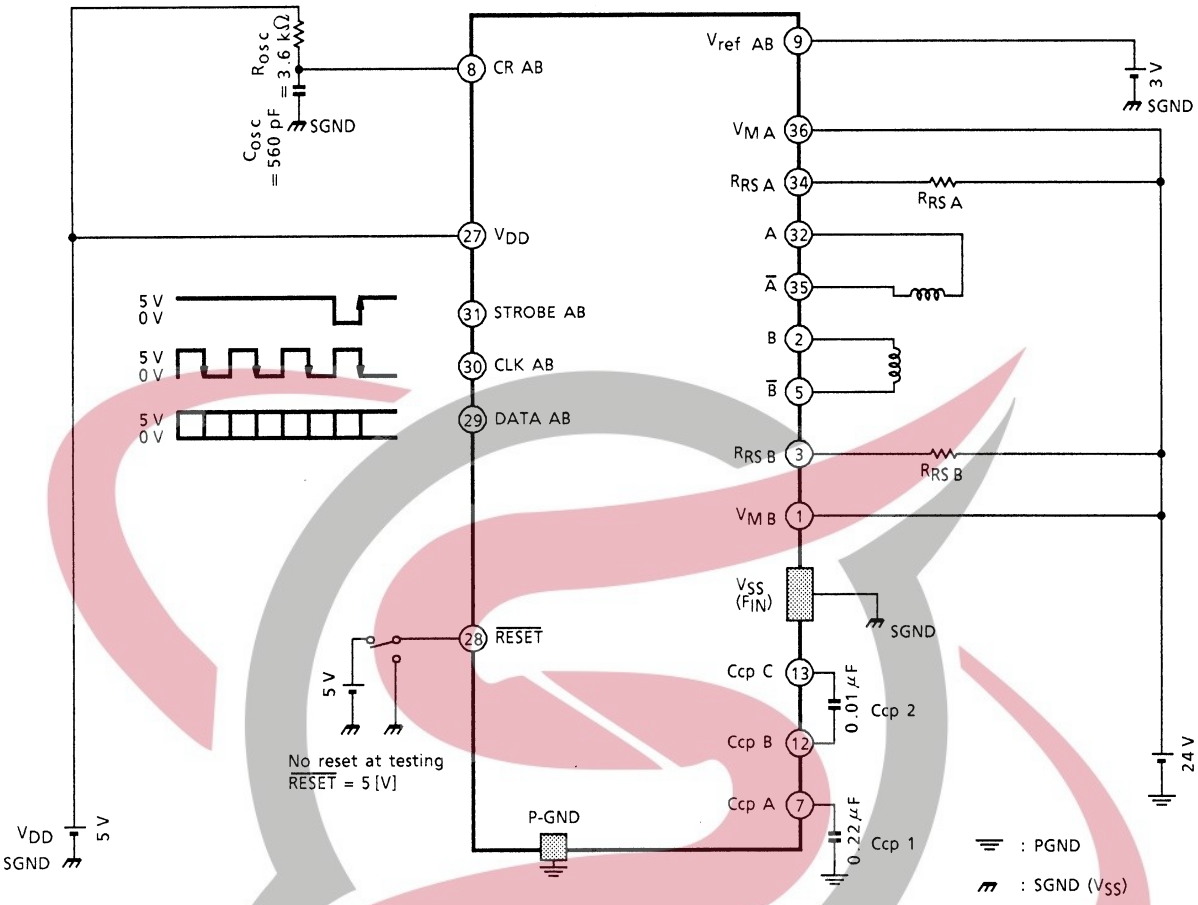
15. Current vector (A/B unit only. C/D unit conforms to A/B unit.)



Perform chopping in Mixed Decay mode with load L. Monitor the output current waveform and measure the output current at constant current operation. At this time, vary the 4-bit data for current setting and measure the current values. Using the set output current as 100%, calculate the output current ratio.

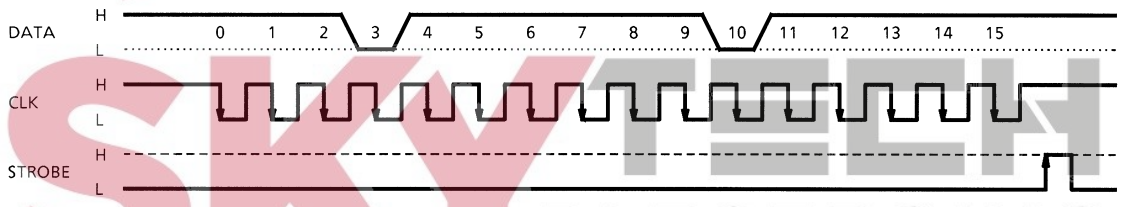


16. f_{CLK}, $t_{w\ (CLK)}$, $t_{wp\ (CLK)}$, $t_{wn\ (CLK)}$, t_{STROBE}, $t_{STROBE\ (H)}$, $t_{STOBE\ (L)}$, $t_{suSIN-CLK}$, $t_{suST-CLK}$, $t_{hSIN-CLK}$, $t_{hCLK-ST}$ (A/B unit only. C/D unit conforms to A/B unit.)

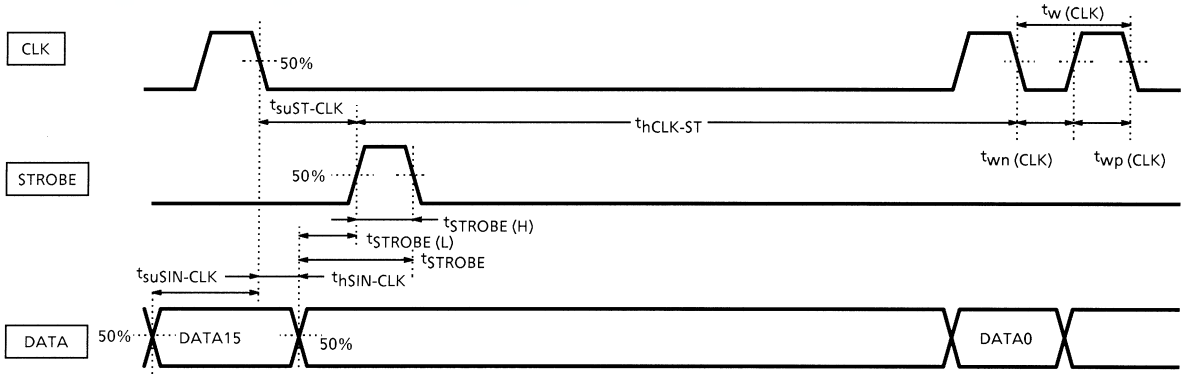


Input any data at f_{CLK} (max), perform chopping, and monitor the output waveform.
For the measuring points, see the timing chart below.

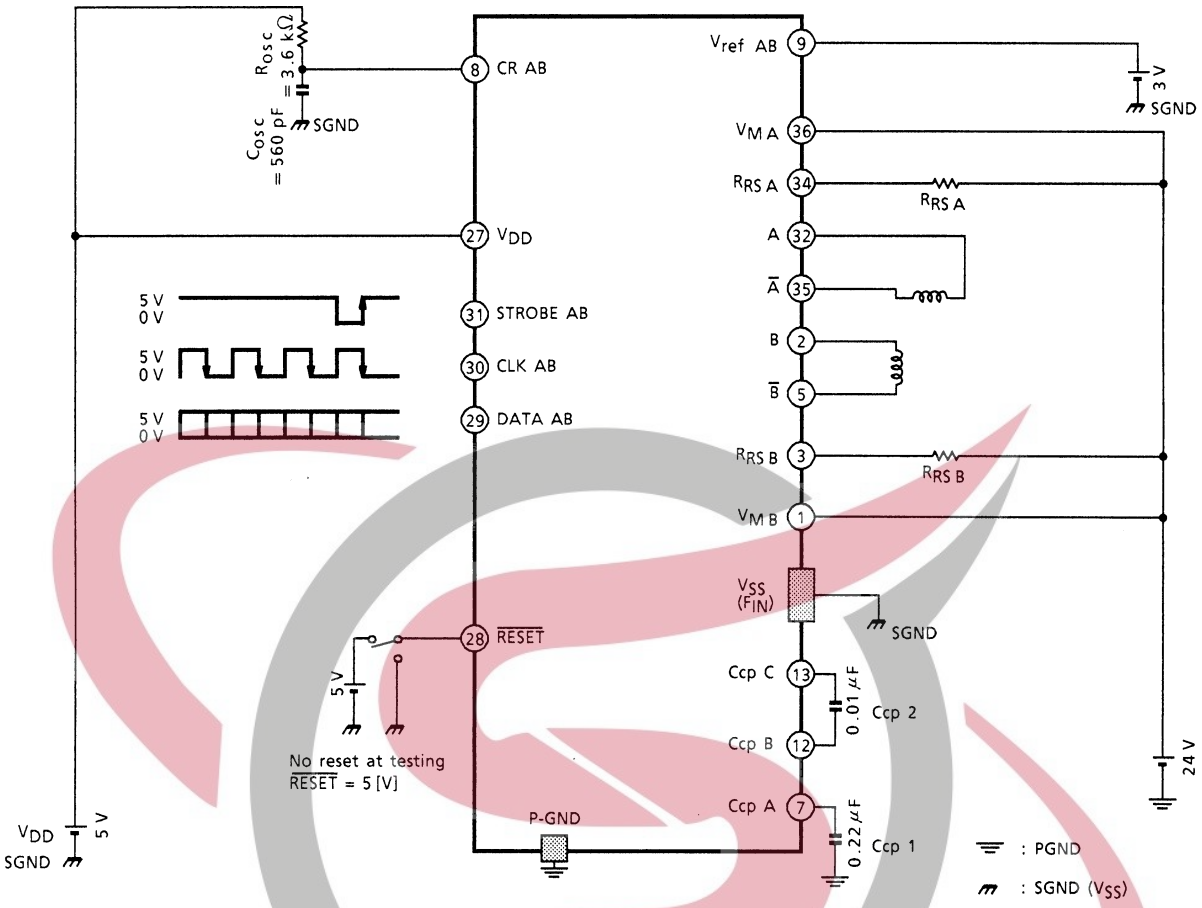
Setup data



Measuring points

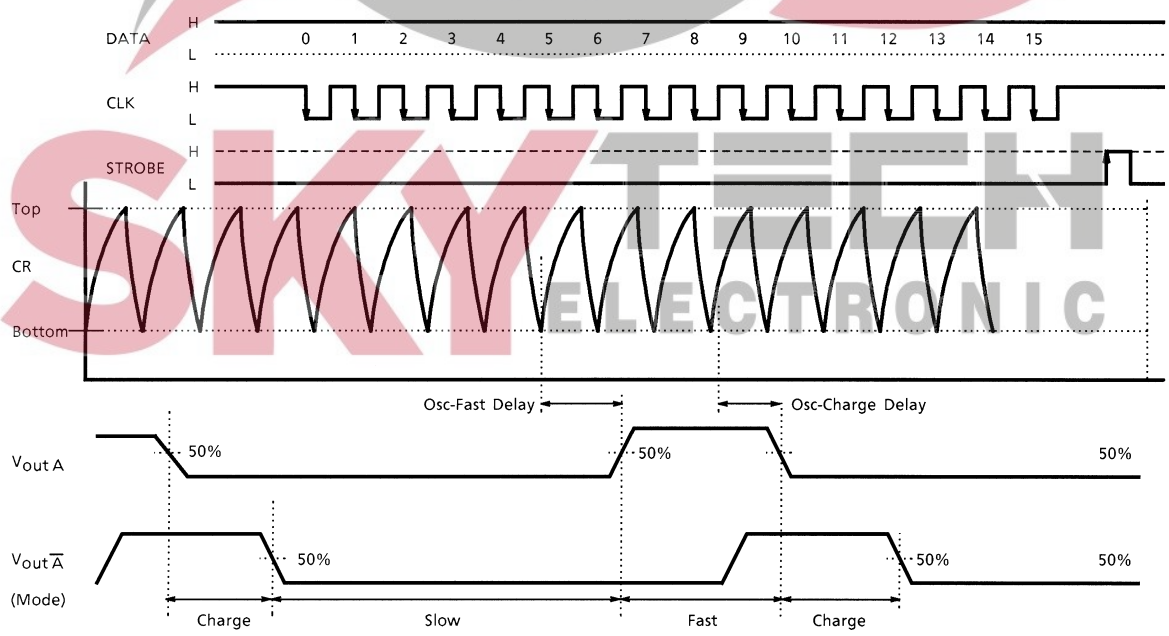


17. OSC-fast delay, OSC-charge delay (A/B unit only. C/D unit conforms to A/B unit.)

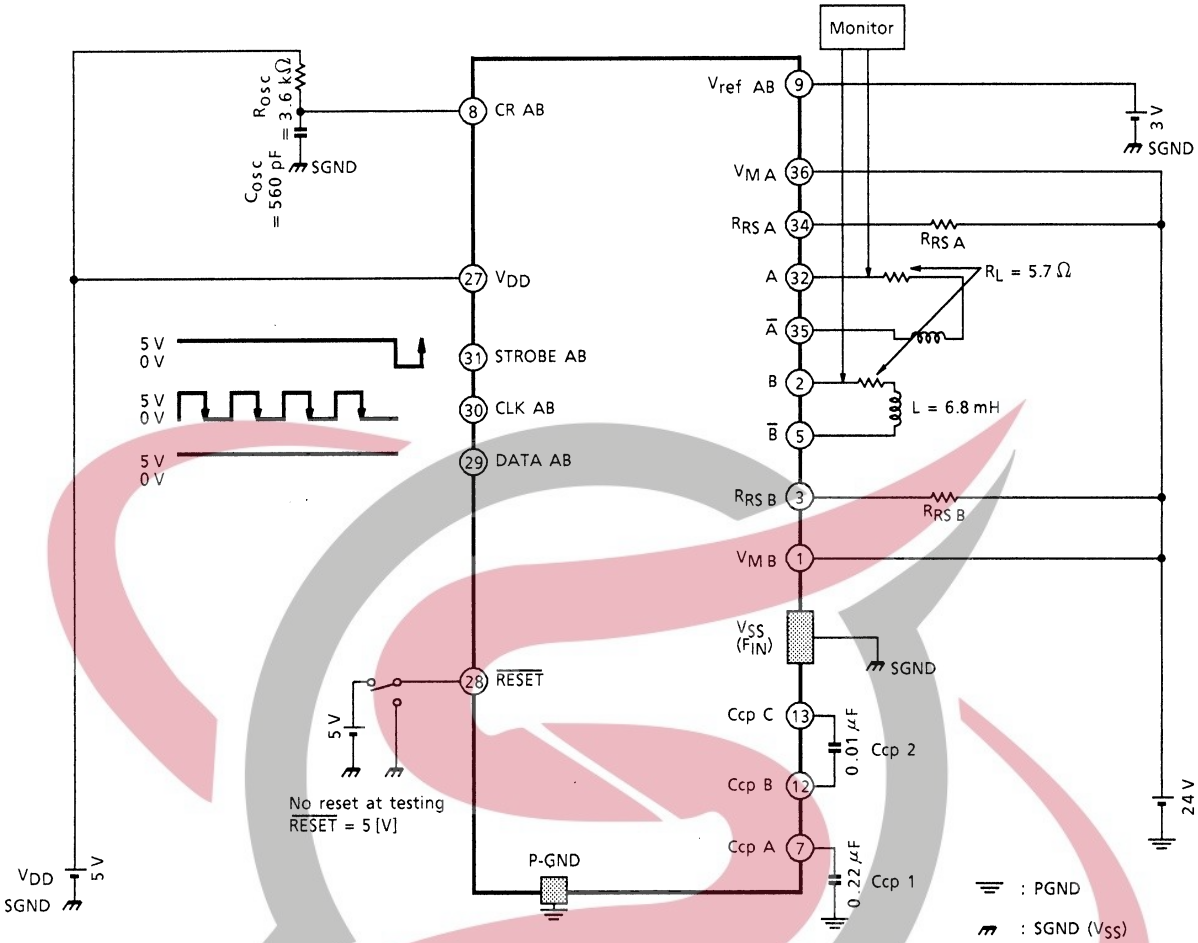


Fix the output current value in Mixed Decay mode and turn the output on. Measure the time until the output switches from the CR pin waveform and the output voltage waveform.

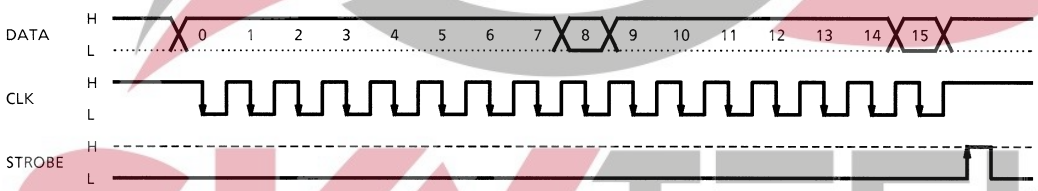
Setup data



18. $t_{pHL\ (ST)}$, $t_{pLH\ (ST)}$, t_r, t_f (A/B unit only. C/D unit conforms to A/B unit.)

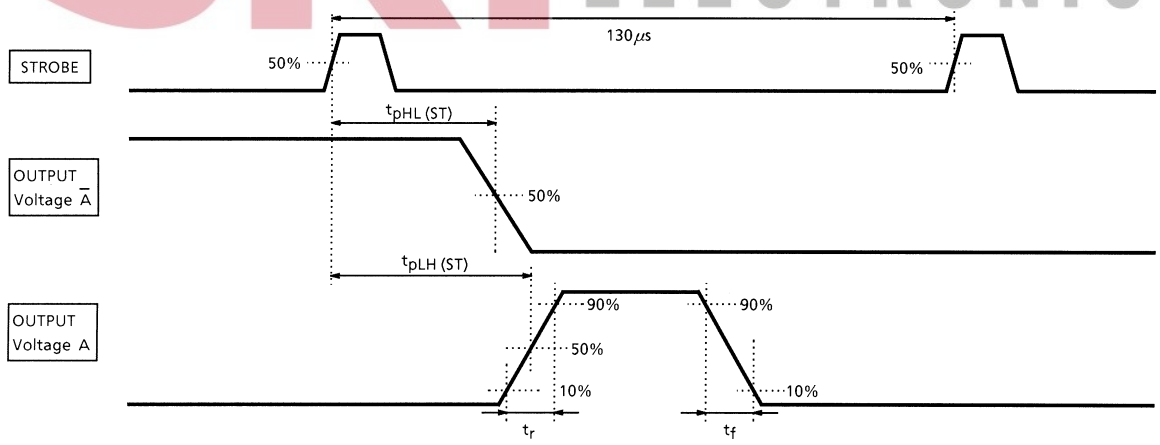


Setup data

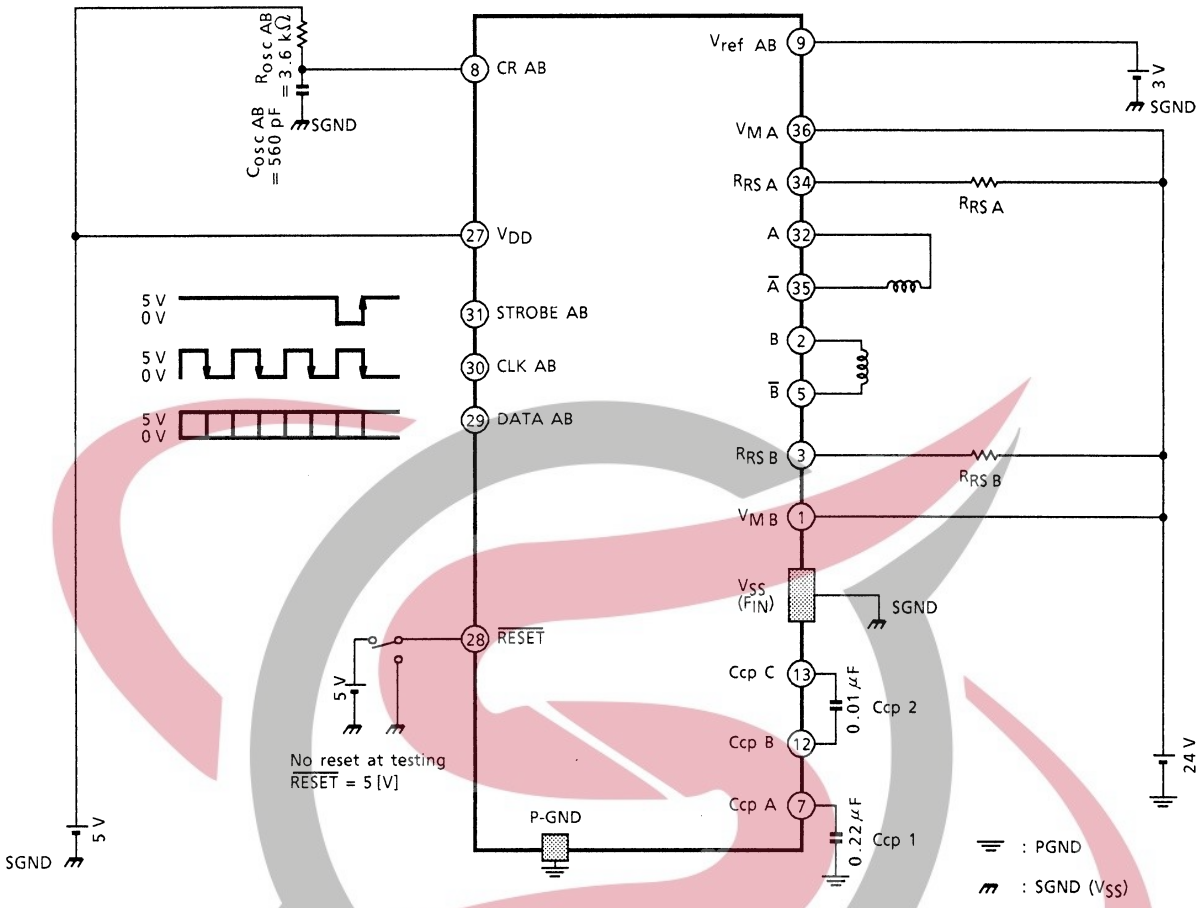


Switch PHASE every 130 μs and measure the output pin voltage and the STROBE signal.

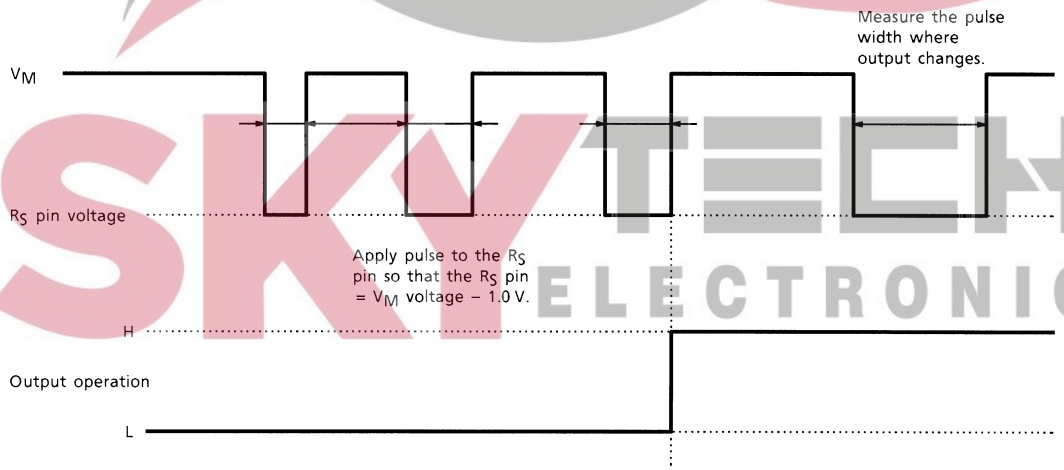
[Oscilloscope waveform (example)]



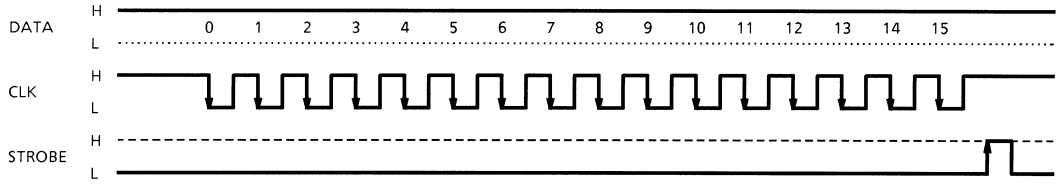
19. t_{BRANK} (A/B unit only. C/D unit conforms to A/B unit.)



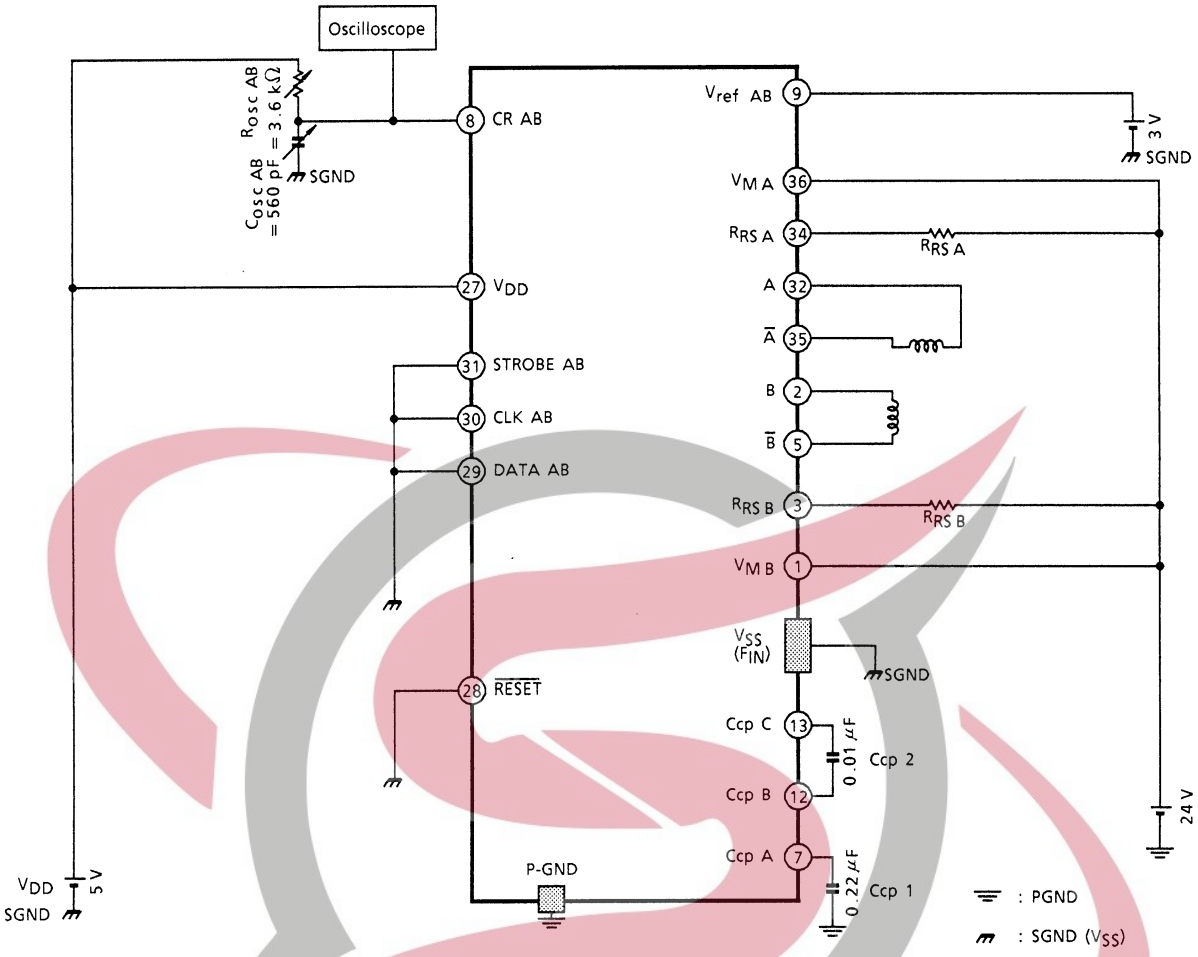
tBRANK is the dead time band for avoiding malfunction caused by noise. Apply sufficient differential voltage (when V_{ref} = 3 V, 0.6 V or higher) to V_M-R_S and apply duty. When the pulse width reaches a certain value, triggering feedback and changing the output. Check the value.



Setup data

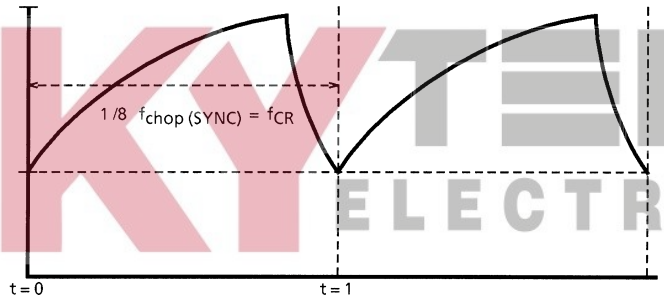


20. f_{chop} (f_{chop} (min), f_{chop} (max)) (A/B unit only. C/D unit conforms to A/B unit.)

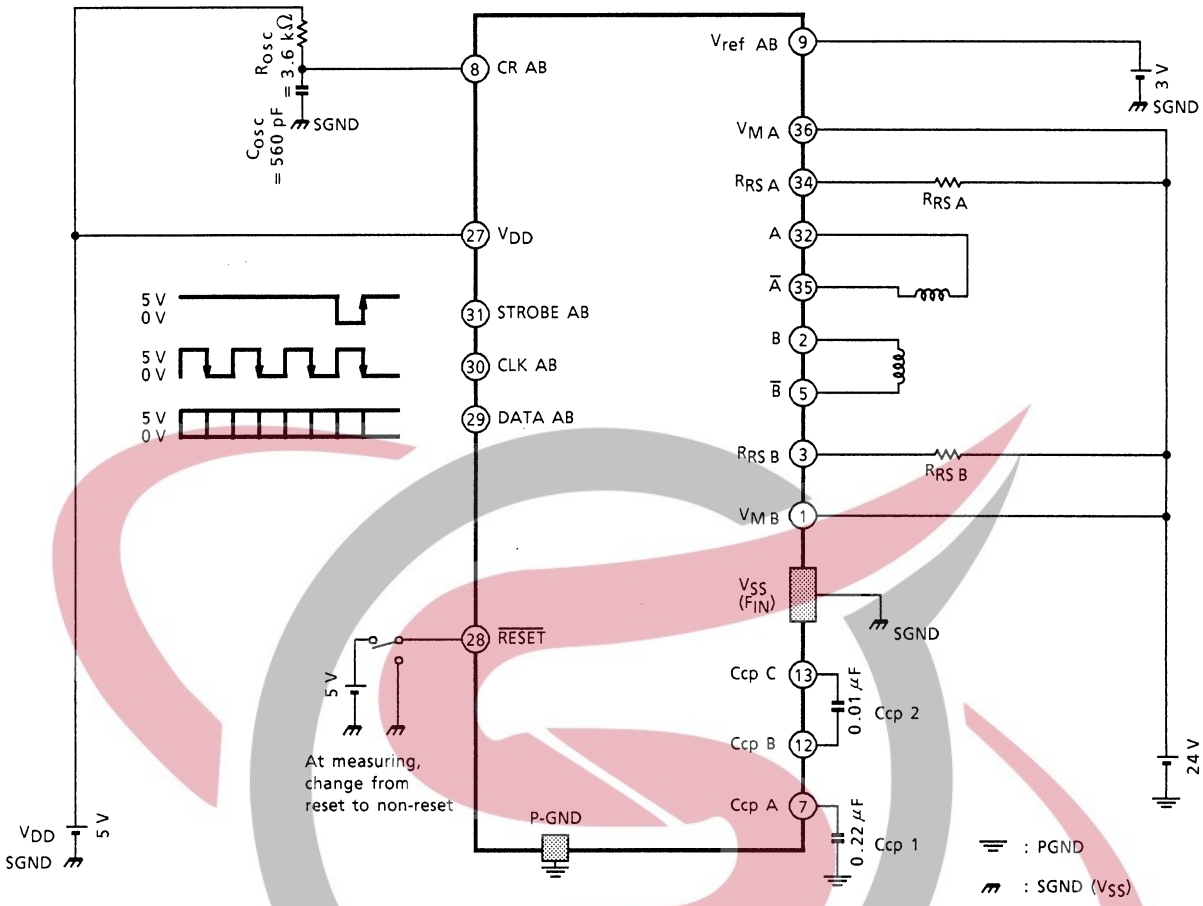


Change the R_{osc} and C_{osc} values and measure the frequency on the CR pin using the oscilloscope. At this time, 1/8 of the frequency of the measured CR waveform is f_{chop}.

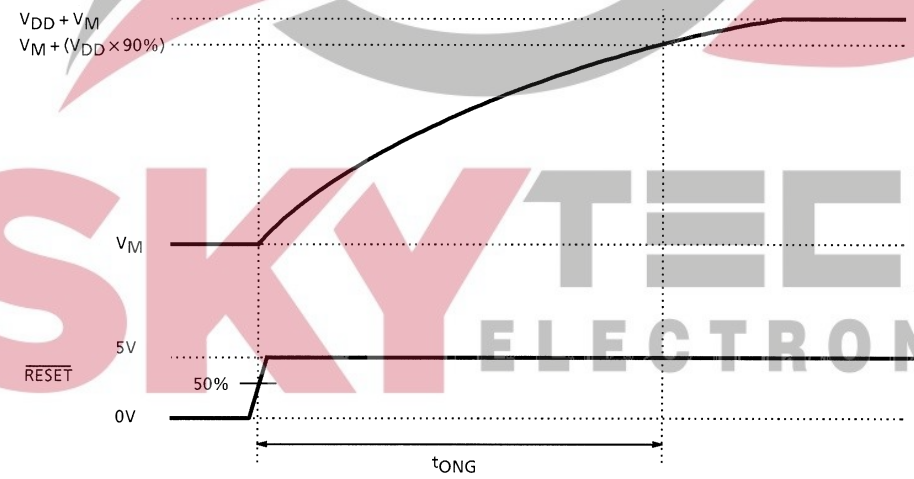
Oscilloscope waveform (example)



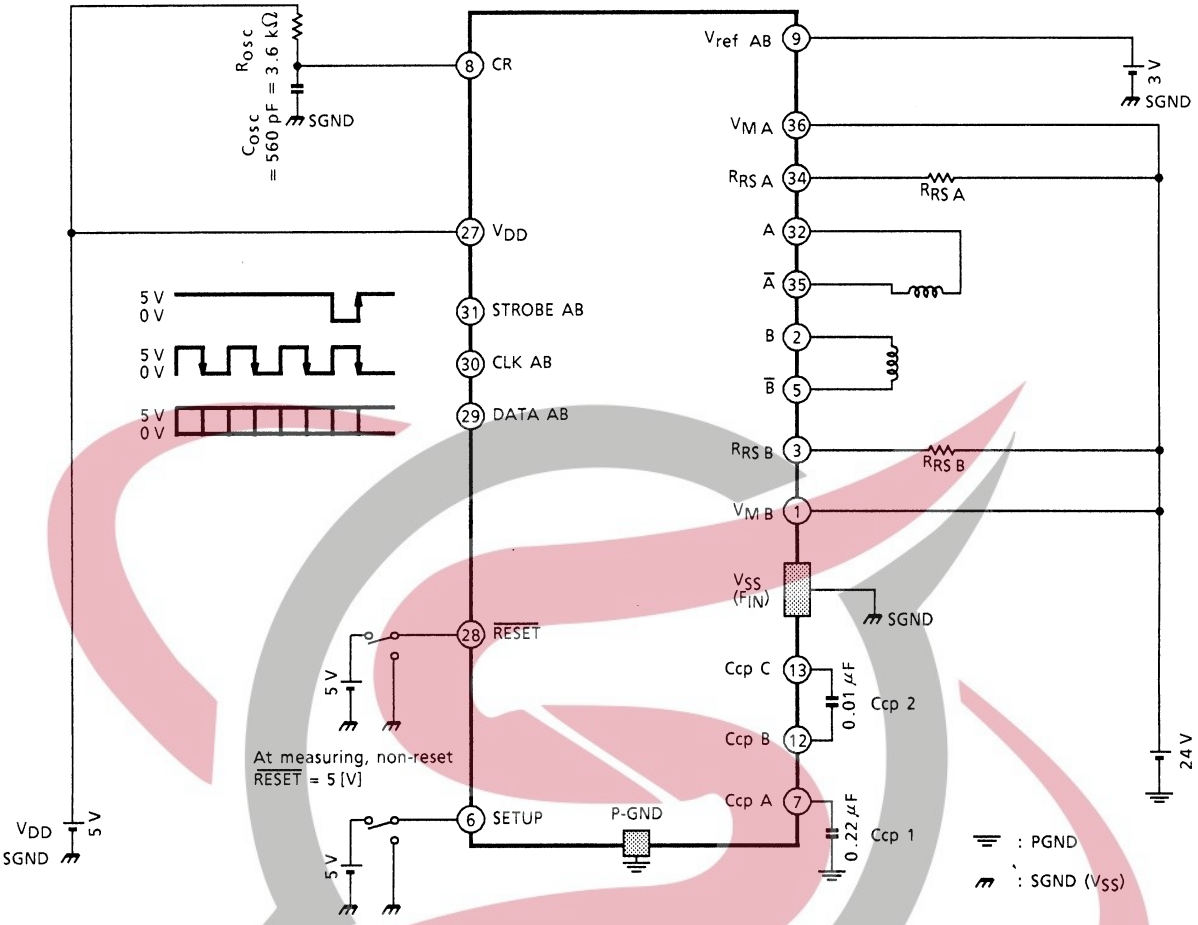
21. t_{ONG} (A/B unit only. C/D unit conforms to A/B unit.)



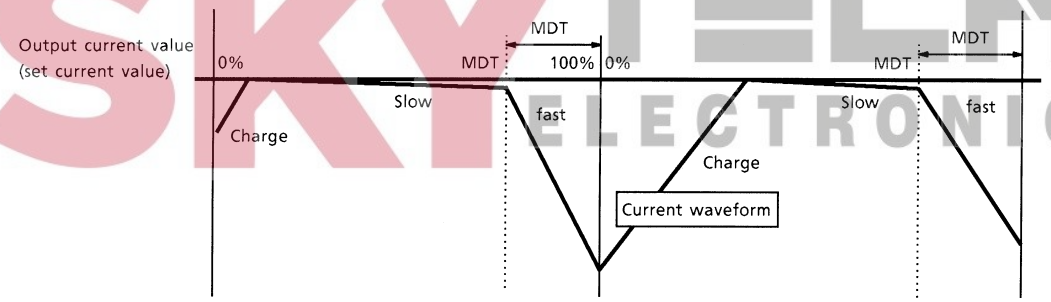
Apply V_M and V_{DD} and change $\overline{RESET}$ from L to H.
Measure the time until the CcpA pin becomes $V_M + V_{DD} \times 90\%$.



22. Mixed decay timming (A/B unit only. C/D unit conforms to A/B unit.)

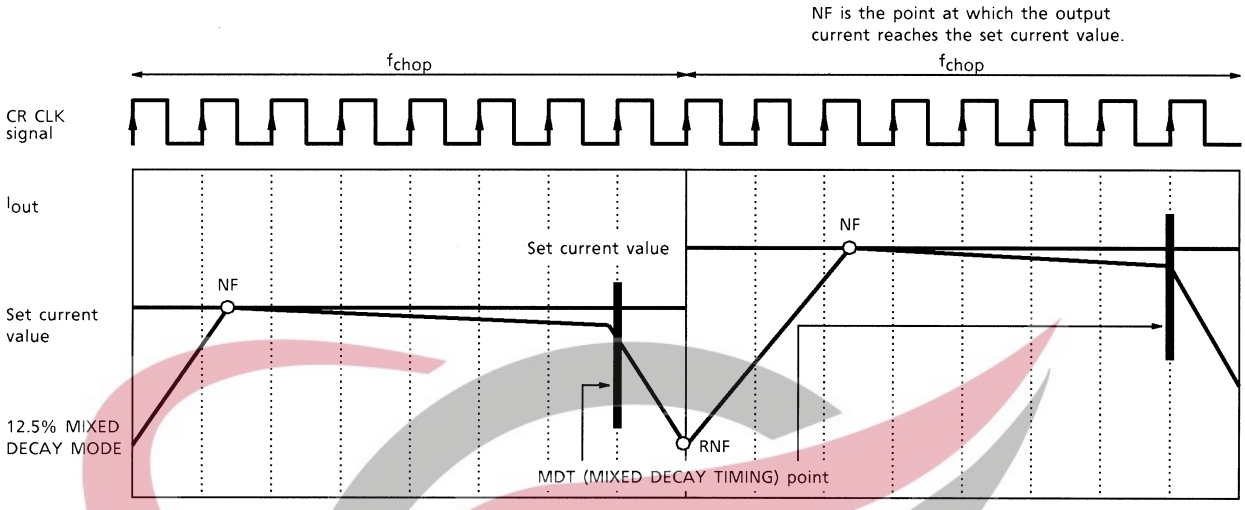


With V_M = 24 V, V_{DD} = 5 V, $\overline{RESET}$ = H, change the SETUP pin from L to H and overwrite the MIXED DECAY TIMING TABLE.
Then change the SETUP pin from H to L. With load L, perform chopping and monitor the output current waveform at that time. Confirm that the switching timing from Slow Decay Mode to Fast Decay Mode within an fchop cycle is the specified MIXED DECAY TIMING.
(Depending on the load L value and the test environment, chopping may be performed every two cycles or there may be no Slow Decay Mode. If so, conditions, for example, load condition, may need to be changed.

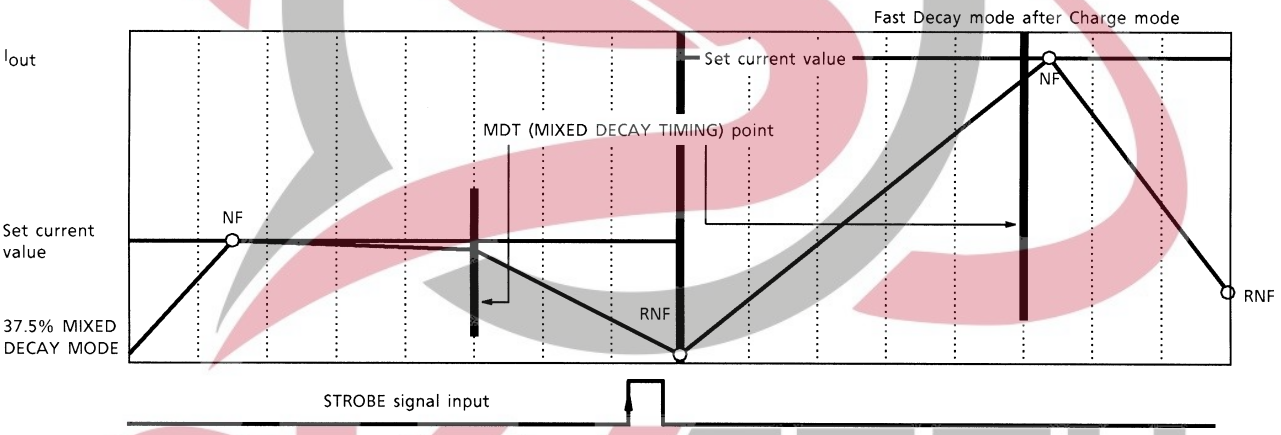


Waveforms in Various Current Modes (Ideal Waveform)

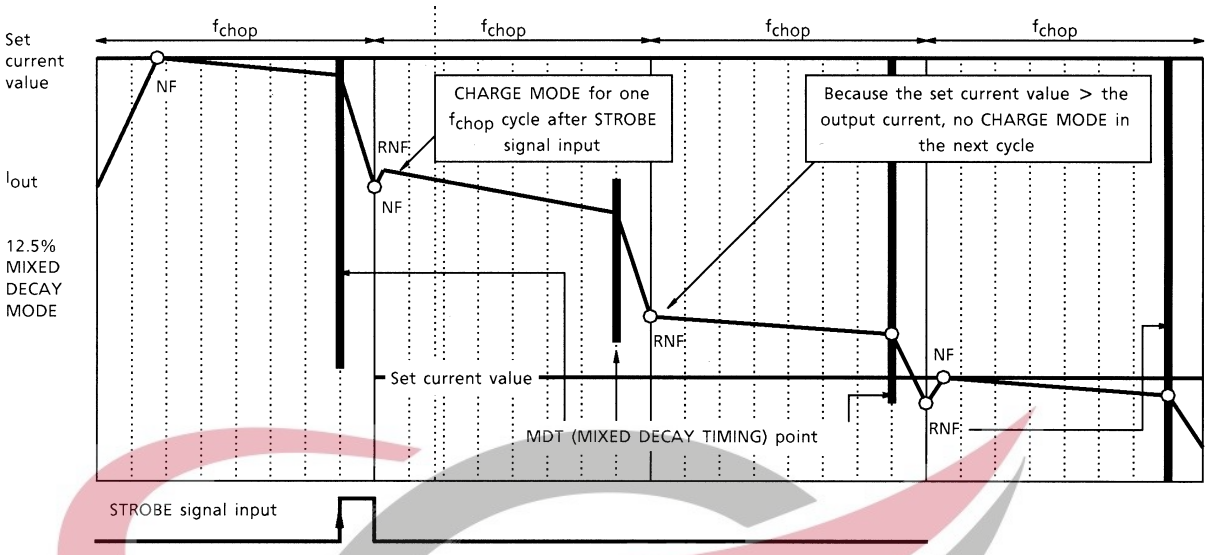
Normal MIXED DECAY MODE Waveform



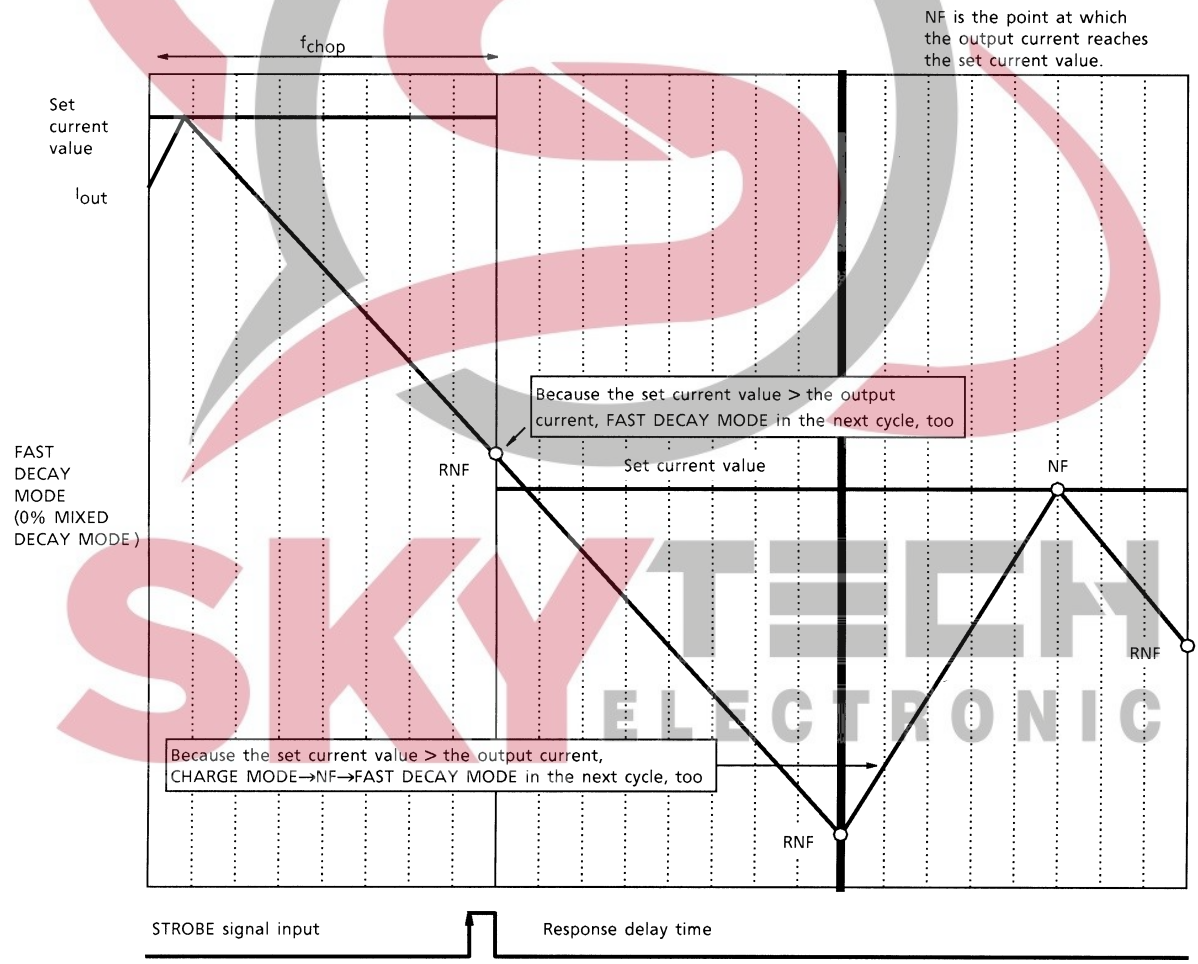
When NF is after MIXED DECAY Timing



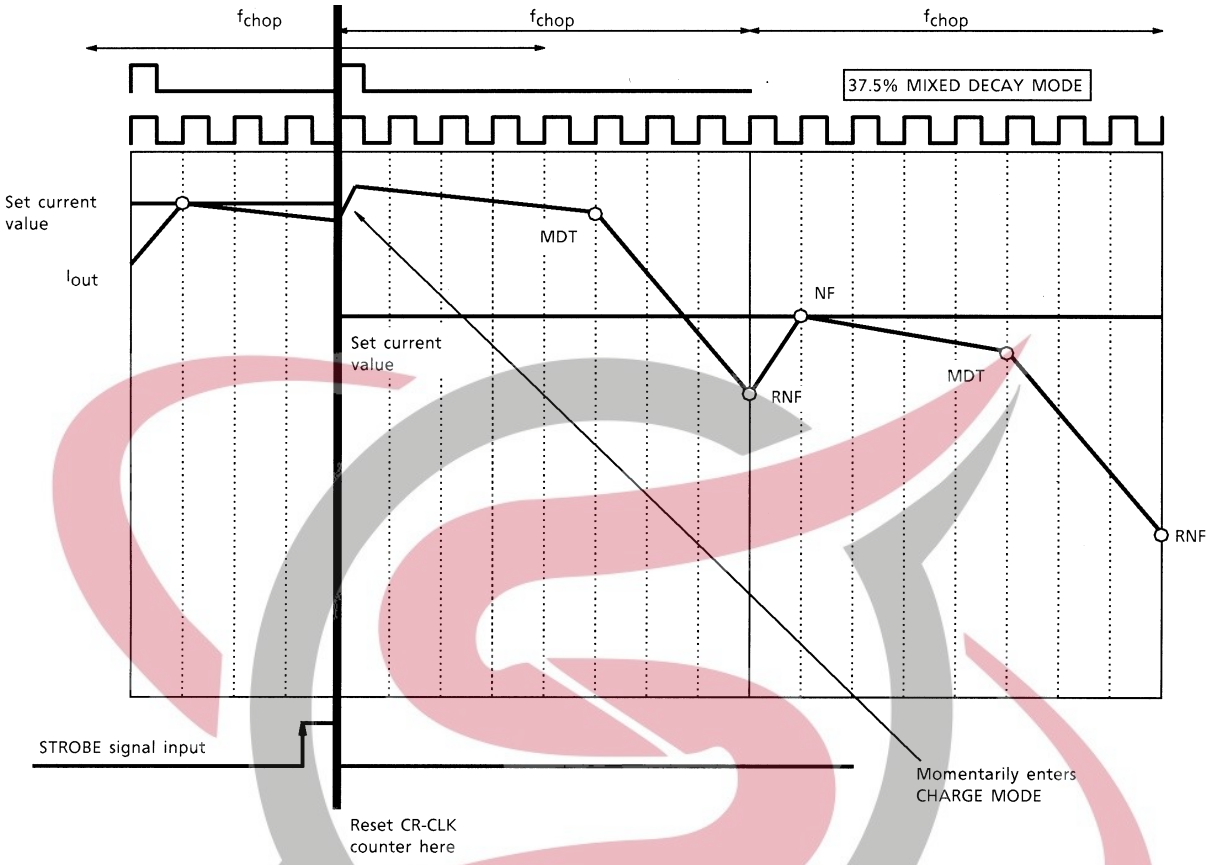
In MIXED DECAY MODE, when the output current > the set current value



FAST DECAY MODE Waveform



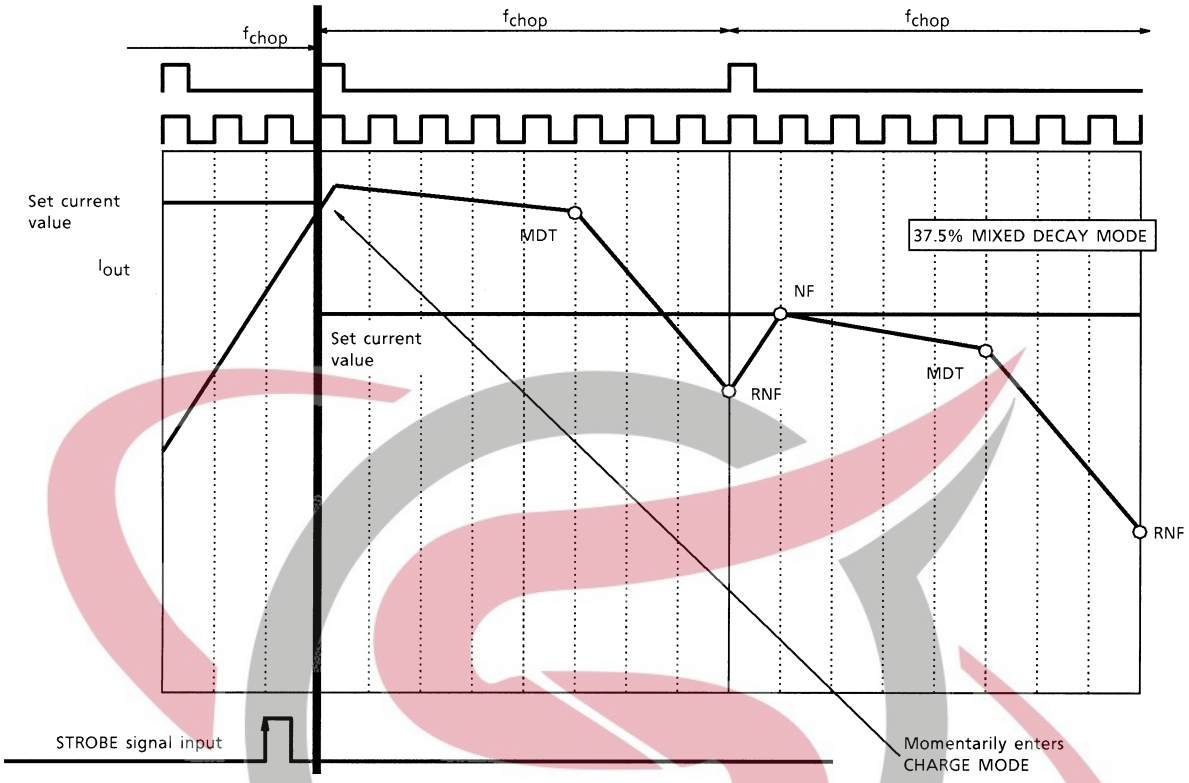
STROBE Signal, Internal CR CLK, and output Current Waveform
(When STROBE Signal is input in SLOW DECAY MODE)



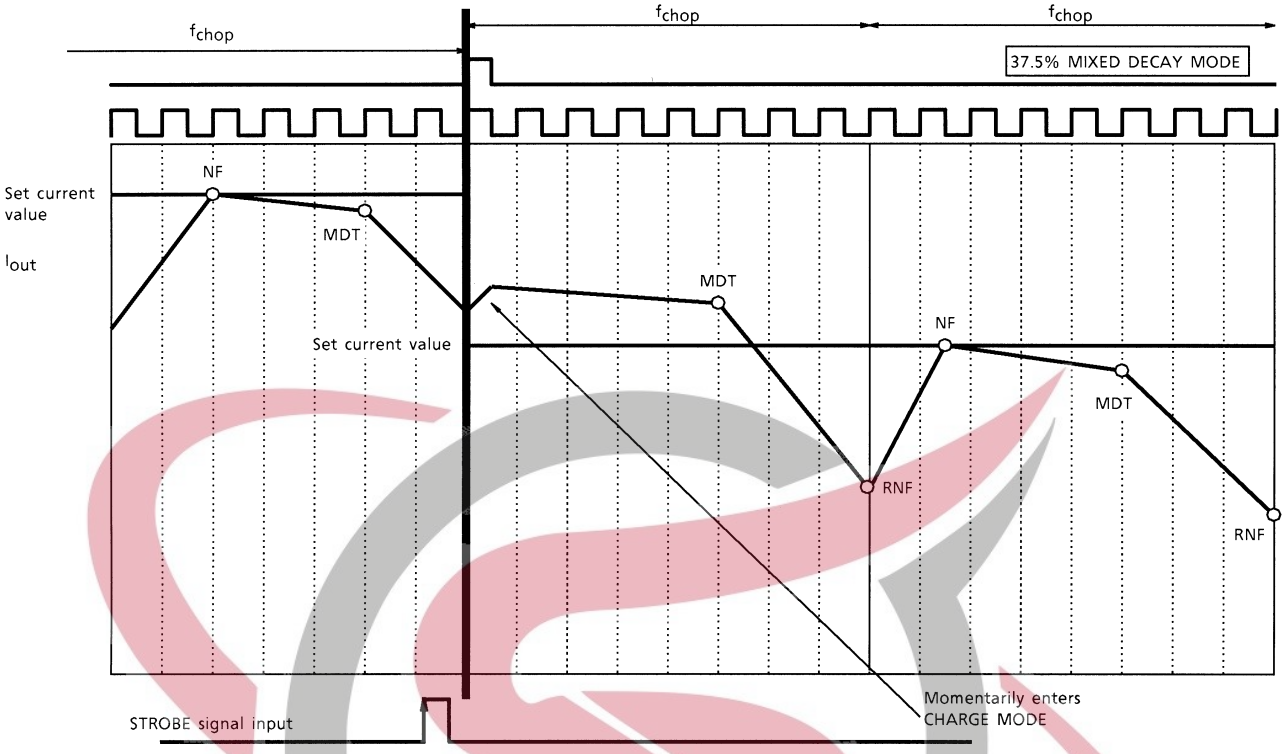
When STROBE signal is input, the chopping counter (CR-CLK counter) is forced to reset at the next CR-CLK timing.
Because of this, compared with a method in which the counter is not reset, response to the input data is faster. (The delay time, the theoretical value in the logic portion, is expected to be a one-cycle CR waveform: 1.25 μS @100 kHz CHOPPING.)
When the CR-CLK counter is reset due to STROBE signal input, CHARGE MODE is entered momentarily due to current comparison.

Note: In FAST DECAY MODE, too, CHARGE MODE is entered momentarily due to current comparison.

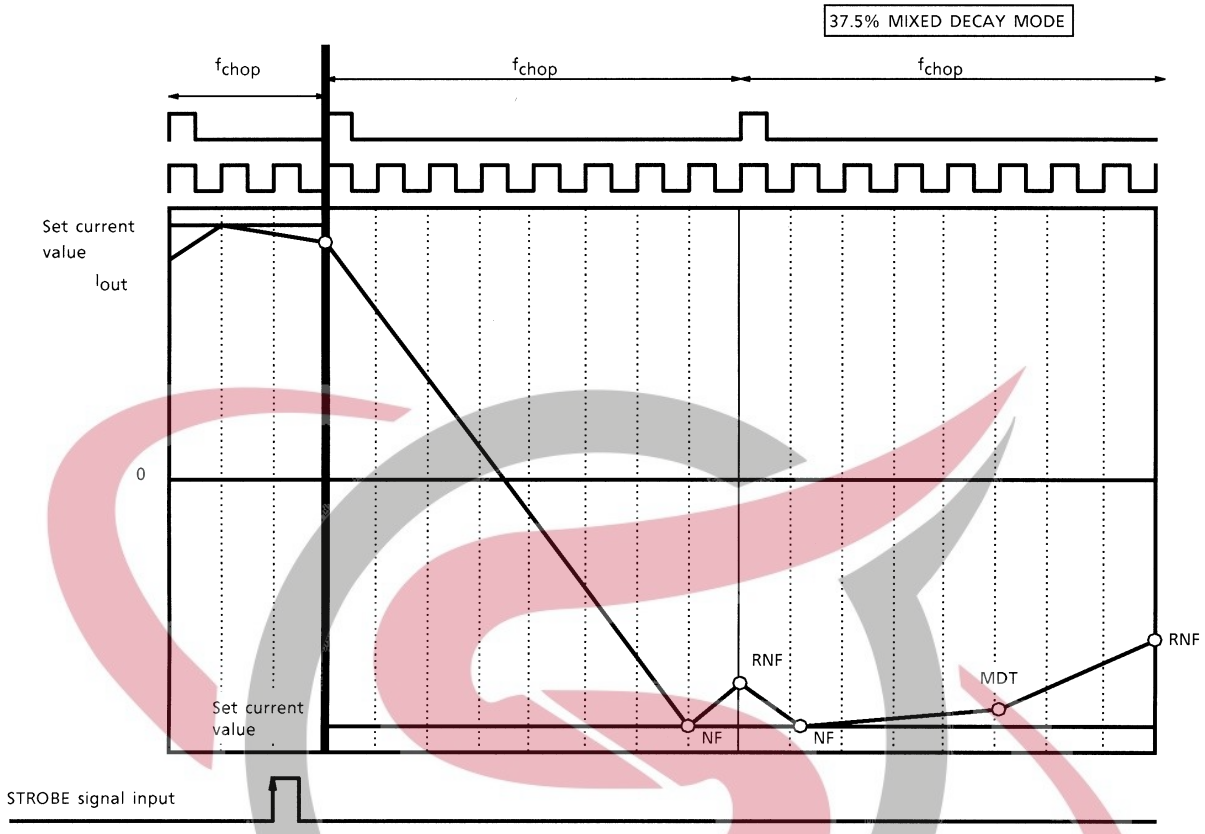
STROBE Signal, Internal CR CLK, and output Current Waveform
(When STROBE signal is input in CHARGE MODE)



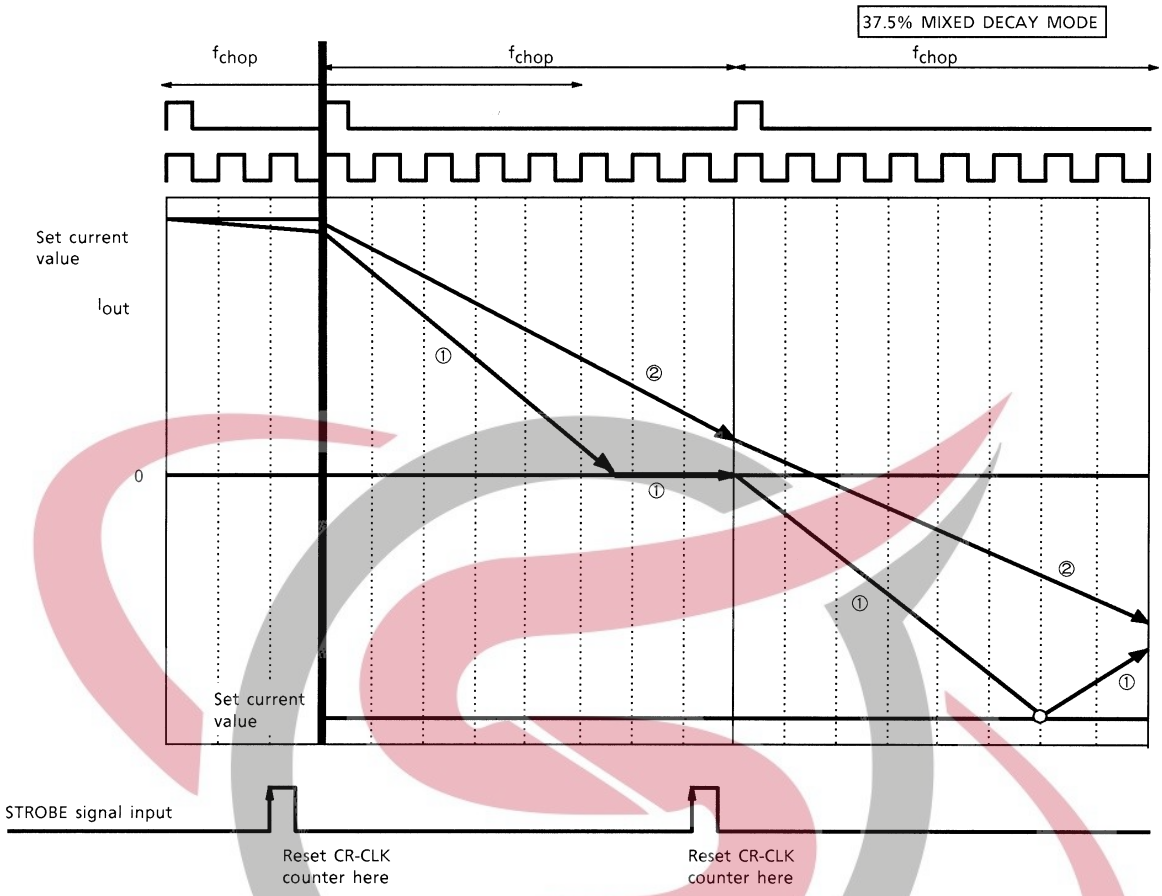
(When STROBE Signal is input in FAST DECAY MODE)



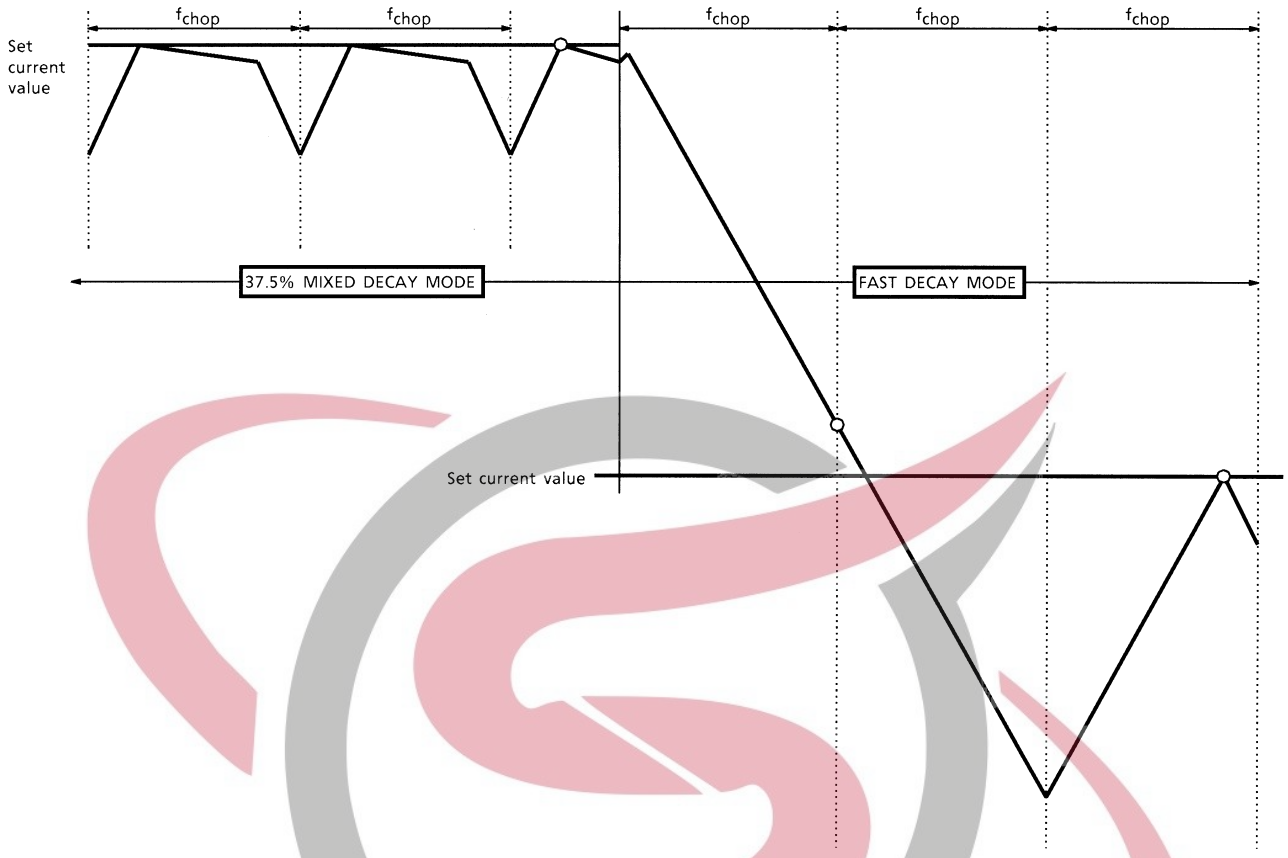
(When PHASE Signal is input)



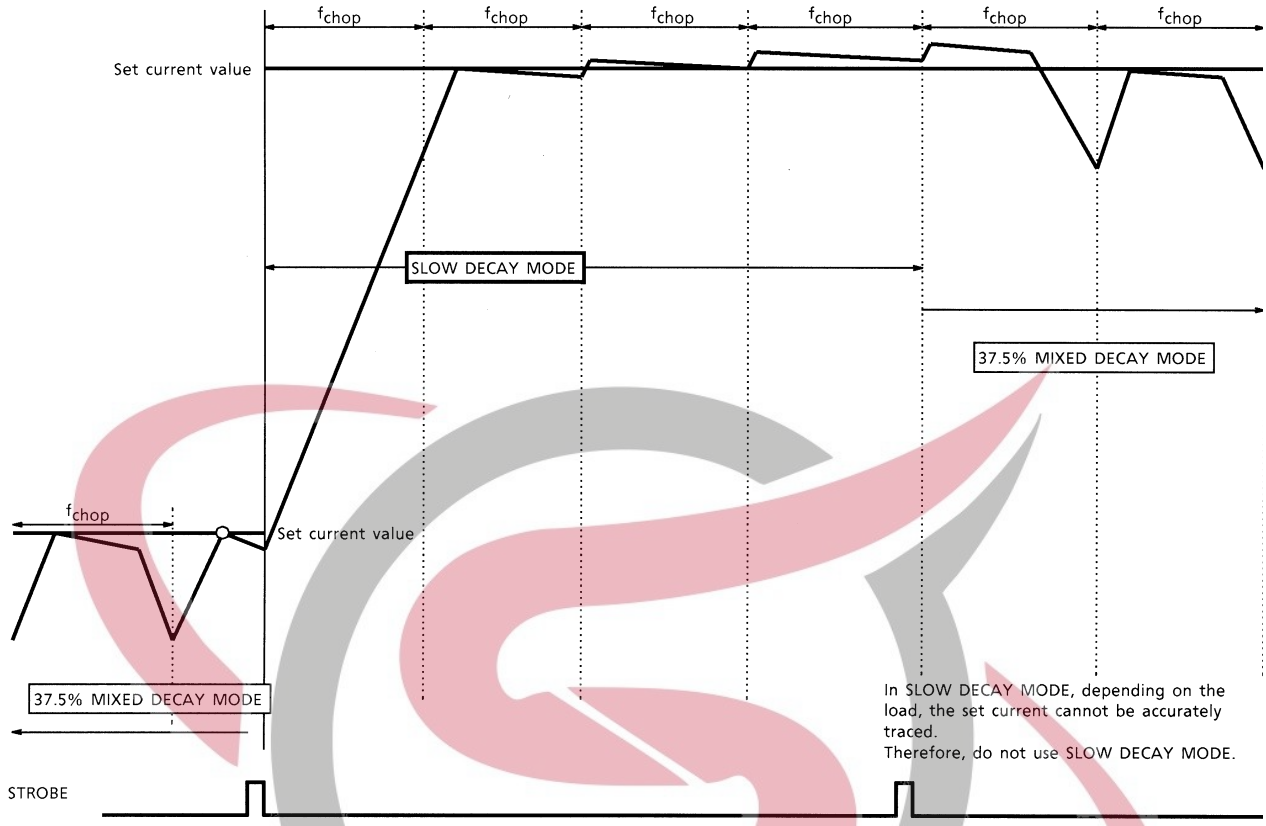
(When current point 0 control is included)



(When FAST DECAY MODE is included during the sequence)

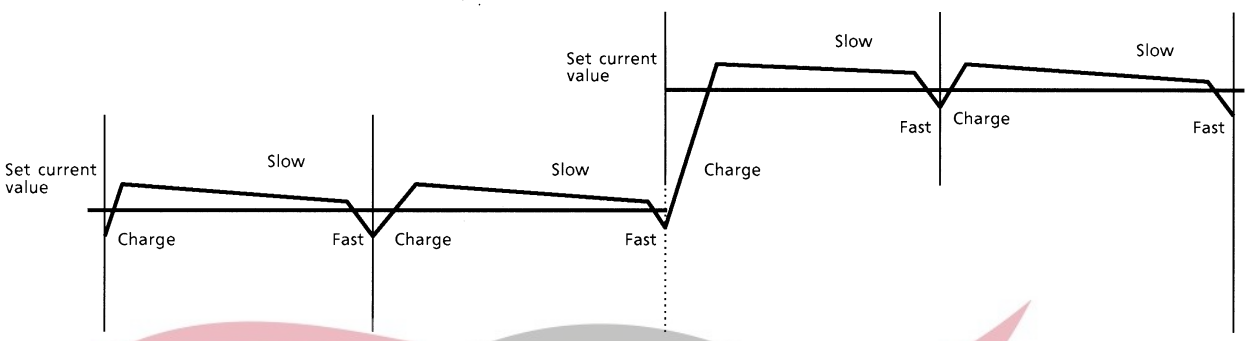


(When SLOW DECAY MODE is included during the sequence)

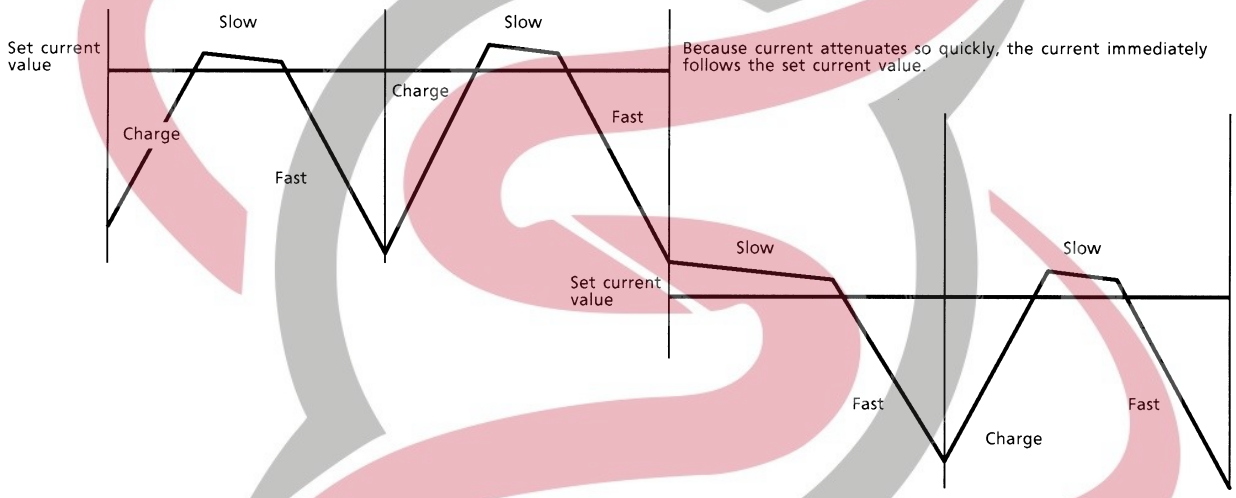


Current Modes
(MIXED (= SLOW + FAST) Decay Mode Effect)

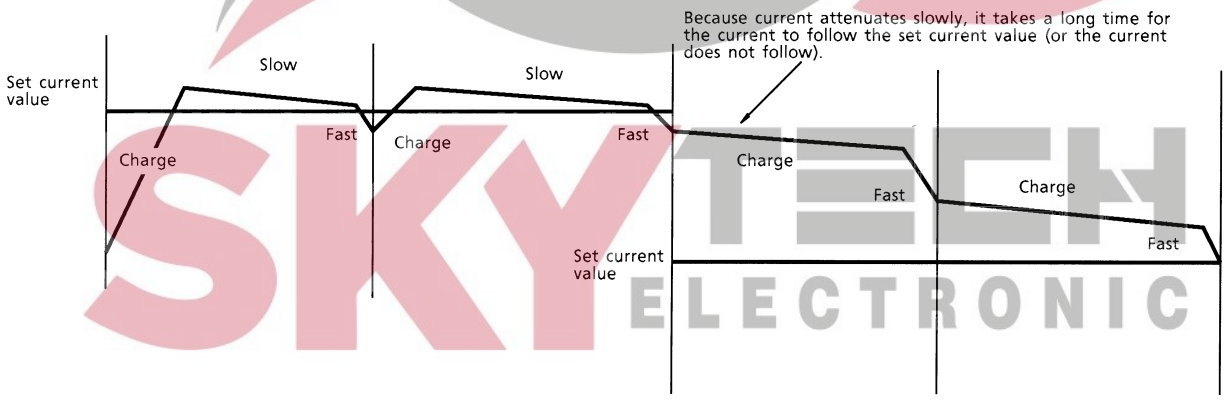
- Sine wave in increasing (Slow Decay Mode (Charge + Slow + Fast) normally used)



- Sine wave in decreasing (When using MIXED DECAY Mode with large attenuation ratio (MDT%) at attenuation)

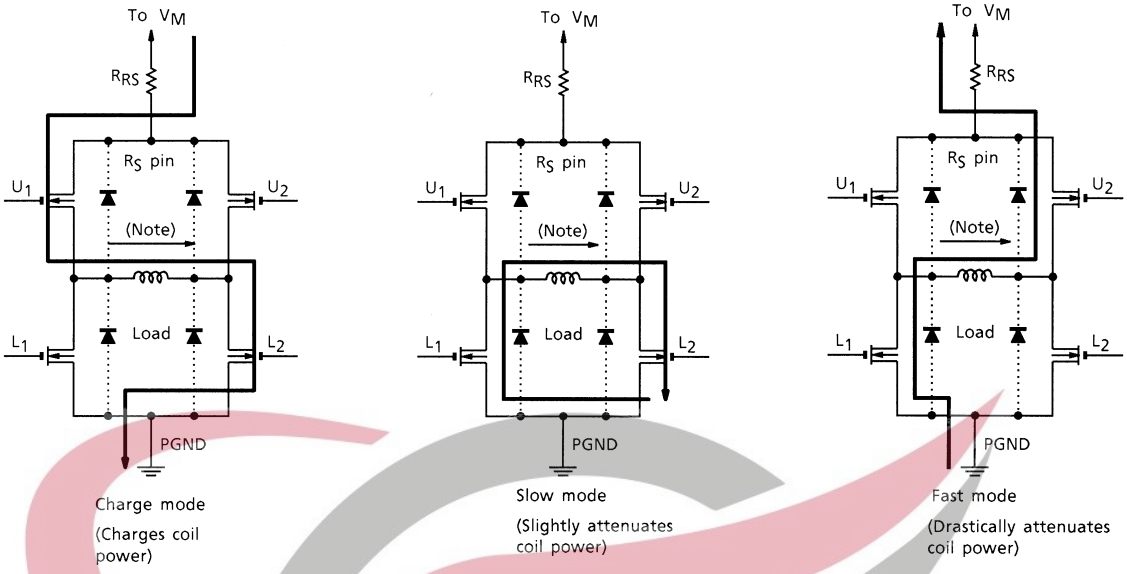


- Sine wave in decreasing (When using MIXED DECAY Mode with small attenuation ratio (MDT%) at attenuation)



Note: The above charts are schematics. The actual current transient responses are curves.

Output Transistor Operating Mode



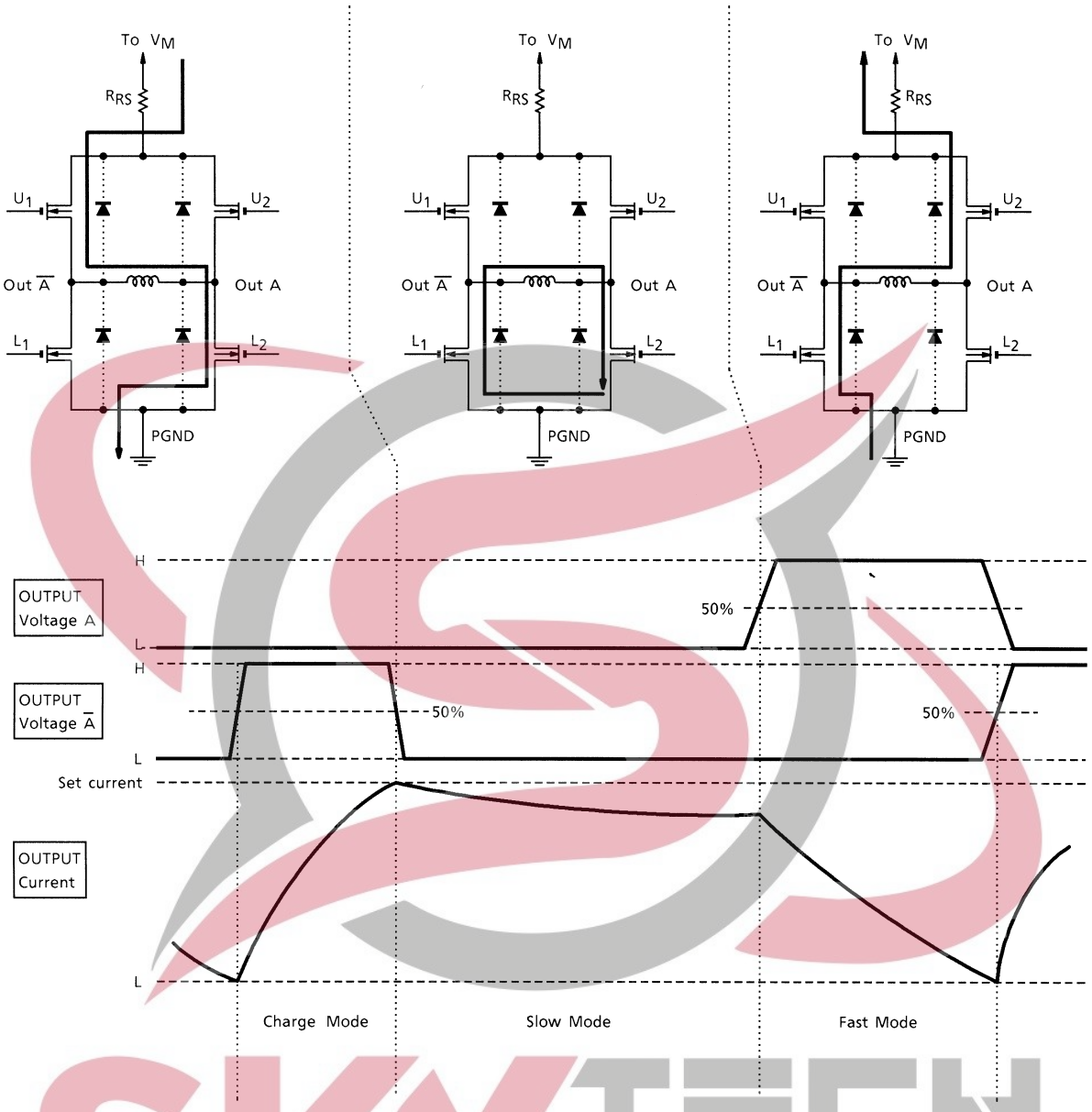
Output Transistor Operation Functions

CLK	U_1	U_2	L_1	L_2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: The above table is an example where current flows in the direction of the arrows in the above figures. When the current flows in the opposite direction of the arrows, see the table below.

CLK	U_1	U_2	L_1	L_2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

Output Transistor Operating Mode 2
(Sequence of MIXED DECAY MODE)

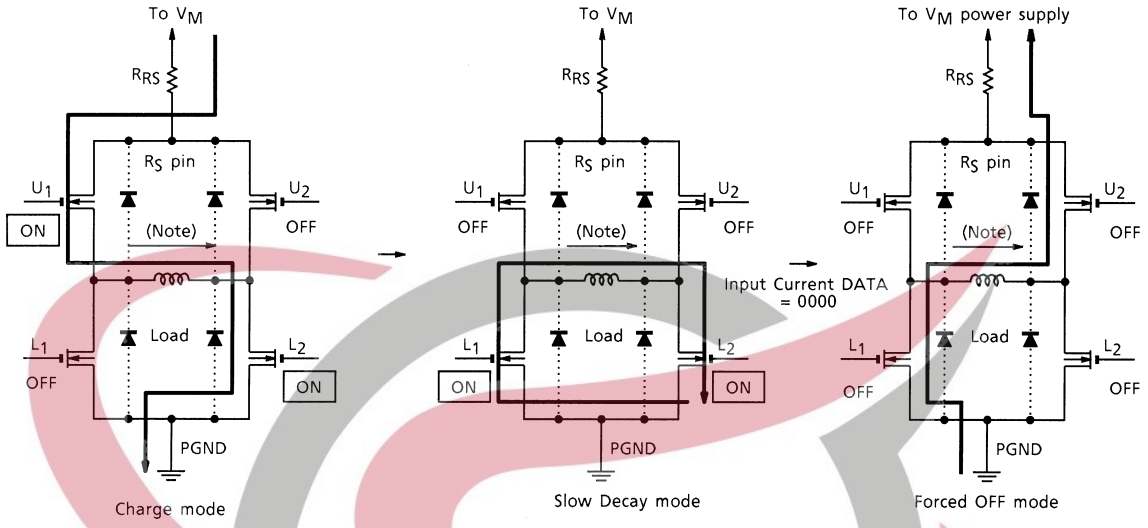


The constant current is controlled by changing mode from Charge → Slow → Fast.

Current Discharge Path when Current Data = 0000 are input during operation

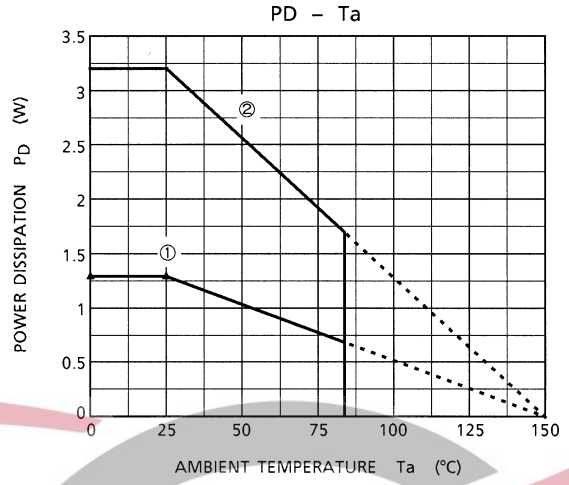
In Slow Decay Mode, when all output transistors are forced to switch off, coil energy is discharged in the following MODES :

Note: Parasitic diodes are located on dotted lines. In normal MIXED DECAY MODE, the current does not flow to the parasitic diodes. However, when signal 0000 is input during operation, the current flows to them.



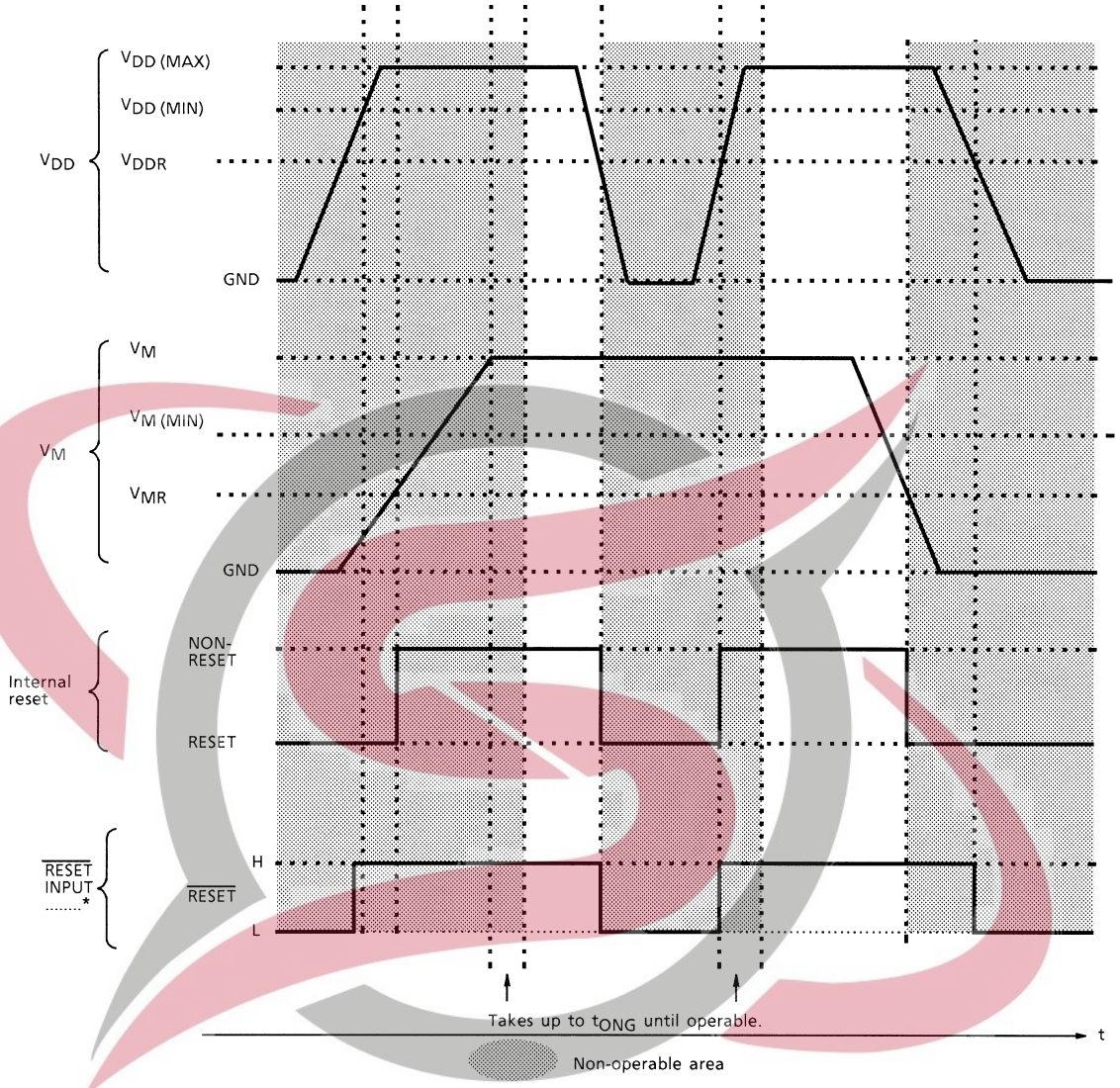
As shown in the figure at right, an output transistor has parasitic diodes.
To discharge energy from the coil, each transistor is switched on allowing current to flow in the reverse direction to that in normal operation. As a result, the parasitic diodes are not used. If all the output transistors are forced to switch off, the energy of the coil is discharged via the parasitic diodes.

PD-Ta (Package Power Dissipation)



① $R_{th\ (j\text{-}a)}$ IC only (96°C / W)
② When mounted on the board (38°C / W)
Board size (100 × 200 × 1.6 mm)
※ $R_{th\ (j\text{-}c)}$: 8.5°C / W

Power Supply Sequence (Recommended)



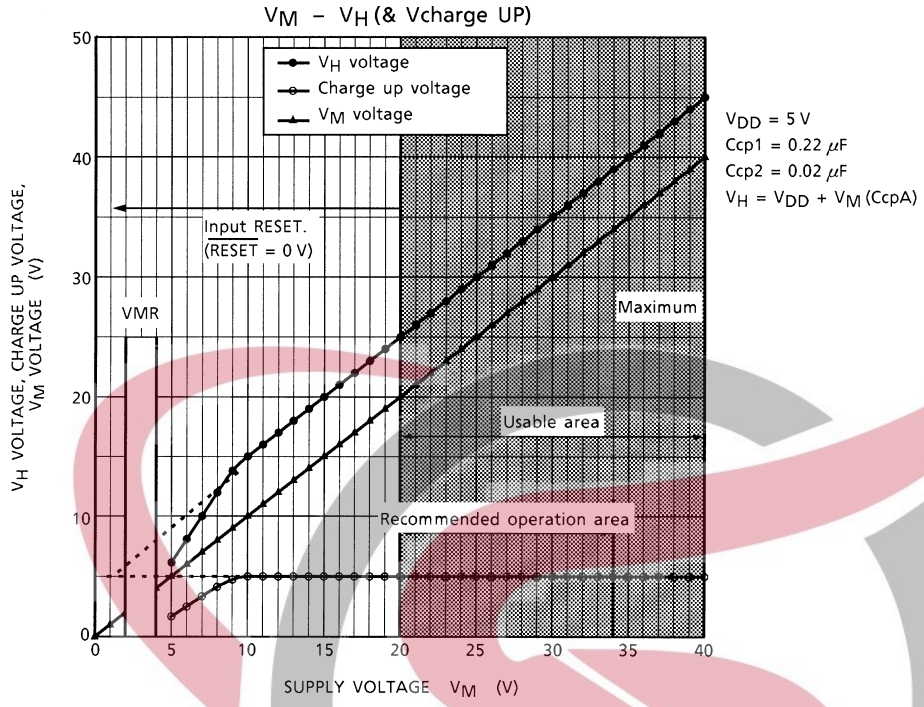
Note 1: If the V_{DD} drops to the level of the V_{DDR} or below while the specified voltage is input to the V_M pin, the IC is internally reset. This is a protective measure against malfunction. Likewise, if the V_M drops to the level of the V_{MR} or below while regulation voltage is input to the V_{DD}, the IC is internally reset as a protective measure against malfunction. To avoid malfunction, when turning on V_M or V_{DD}, we recommend you input the $\overline{\text{RESET}}$ signal at the above timing.
It takes time for the output control charge pump circuit to stabilize. Wait up to t_{ONG} time after power on before driving the motors.

Note 2: When the V_M value is between 3.3 to 5.5 V, the internal reset is released, thus output may be on. In such a case, the charge pump cannot drive stably because of insufficient voltage. We recommend the RESET state be maintained until V_M reaches 20 V or more.

Note 3: Since V_{DD} = 0 V and V_M = voltage within the rating are applied, output is turned off by internal reset. At that time, a current of several mA flows due to the Pass between V_M and V_{DD}.

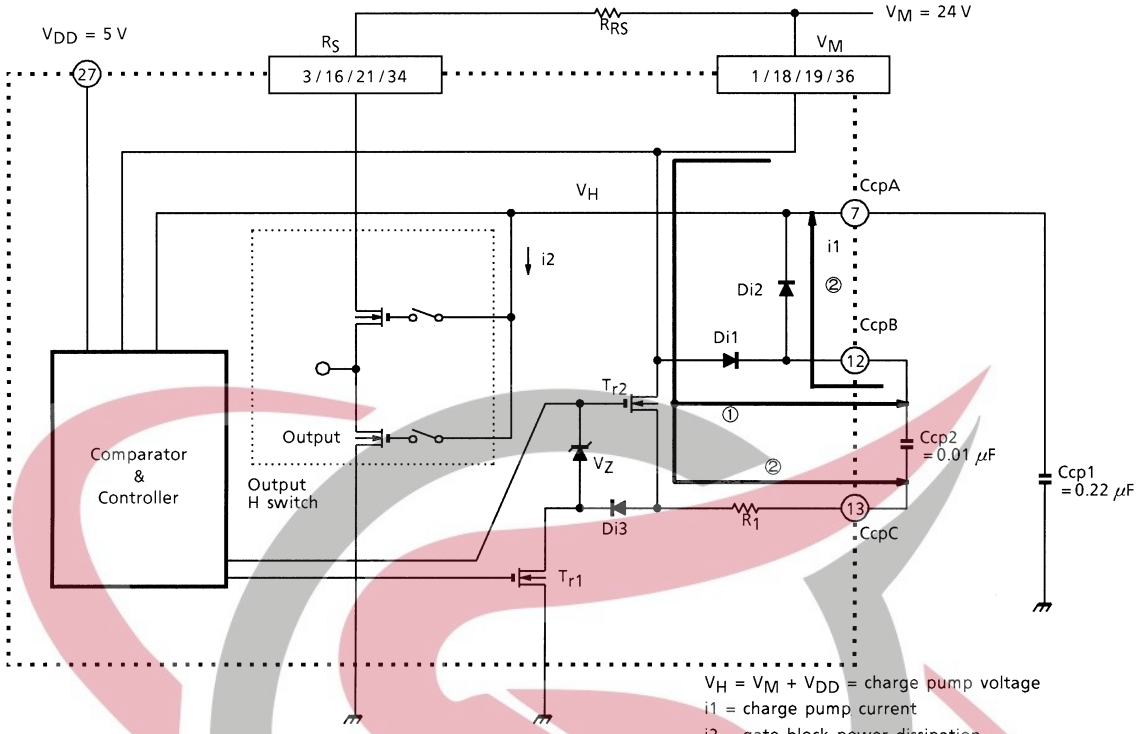
Relationship between V_M and V_H

V_H is the voltage of the CcpA pin. It is the highest voltage in this IC (power supply for driving the upper gate of the H bridge).



- V charge Up is the voltage to boost V_M to V_H. Usually equivalent to V_{DD}.

Operation of Charge Pump Circuit



- Initial charging

(1) When RESET is released, T_{r1} is turned ON and T_{r2} turned OFF. Ccp2 is charged from Ccp2 via Di1 (This is the same as when TSD and ISD are operating and the IC is restored from Reset state.)

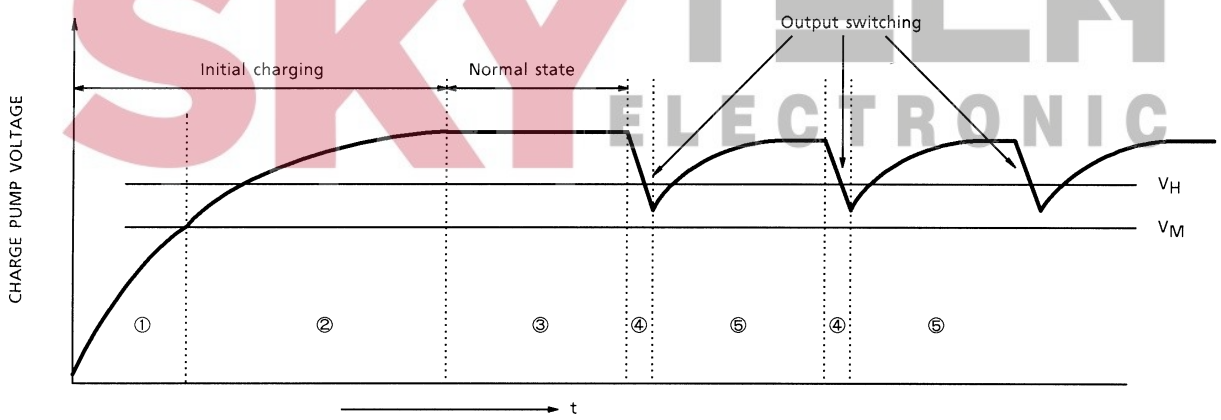
(2) T_{r1} is turned OFF, T_{r2} is turned ON, and Ccp1 is charged from Ccp2 via Di2.

(3) When the voltage difference between V_M and V_H (CcpA pin voltage = charge pump voltage) reaches V_{DD} or higher, operation halts (Steady state : Because the capacitor is naturally discharged, the IC is continually charging to the capacitor).

- Actual operation

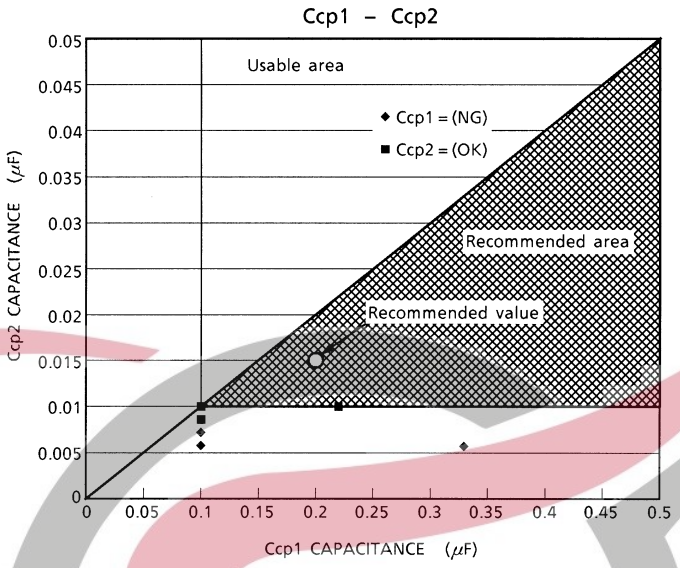
(4) Ccp1 charge is used at fchop switching and the V_H potential drops.

(5) Charges up by (1) and (2) above.



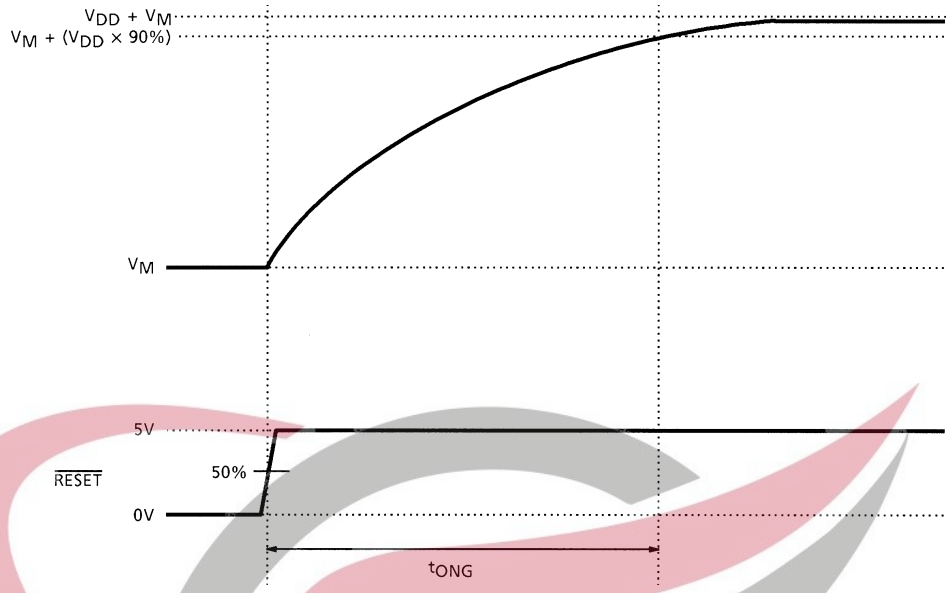
External Capacitors for Charge Pumps

When V_{DD} = 5V, fchop = 100 kHz, and L = 10 mH is driven with V_M = 24 V, I_{out} = 1100 mA, the theoretical values for Ccp1 and Ccp2 are as shown below:



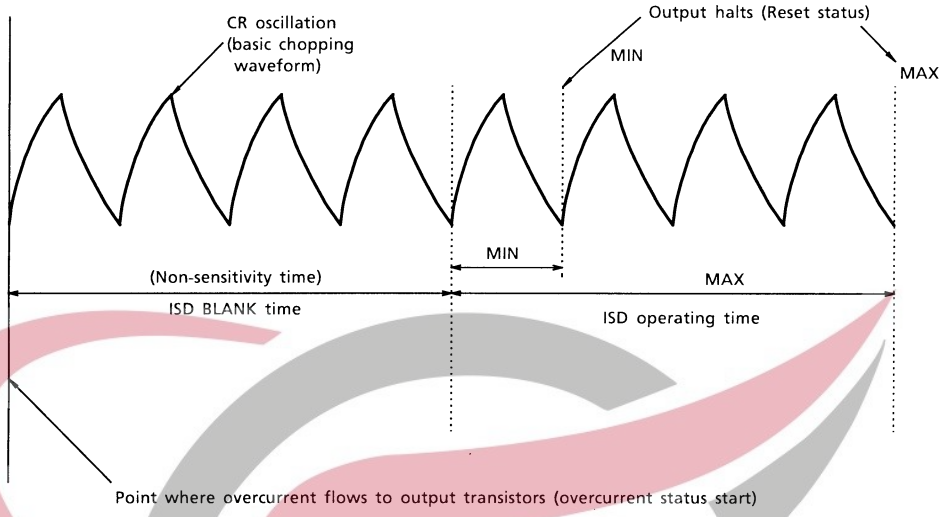
Combine Ccp1 and Ccp2 as shown in the shaded area in the above graph.
Select values 10: 1 or more for Ccp1: Ccp2.
When making a setting, evaluate properly and set values with a margin.

Charge Pump Rise Time



t_{ONG}: Time taken for capacitor Ccp2 (charging capacitor) to fill up Ccp1 (capacitor used to save charge) to $V_M + V_{DD}$ after a reset is released.
The internal IC cannot drive the gates correctly until the voltage of Ccp1 reaches $V_M + V_{DD}$. Be sure to wait for t_{ONG} or longer before driving the motors.
Basically, the larger the Ccp1 capacitance, the longer the initial charge-up time but the smaller the voltage fluctuation.
The smaller the Ccp1 capacitance, the shorter the initial charge-up time but the larger the voltage fluctuation.
Depending on the combination of capacitors (especially with small capacitance), voltage may not be sufficiently boosted. Thus, use the capacitors under the capacitor combination conditions (Ccp1 = 0.22 μF, Ccp2 = 0.01 μF) recommended by Toshiba.

Operating Time for Overcurrent Protector Circuit
(ISD non-sensitivity time and ISD operating time)



A non-sensitivity time is set for the overcurrent protector circuit to avoid misdetection of overcurrent due to spike current at irr or switching.
The non-sensitivity time synchronizes with the frequency of the CR for setting the chopping frequency. The non-sensitivity time is set as follows :

Non-sensitivity time = 4 × CR cycle

The time required for the ISD to actually operate after the non-sensitivity time is as follows :

Minimum: 5 × CR cycle
Maximum: 8 × CR cycle

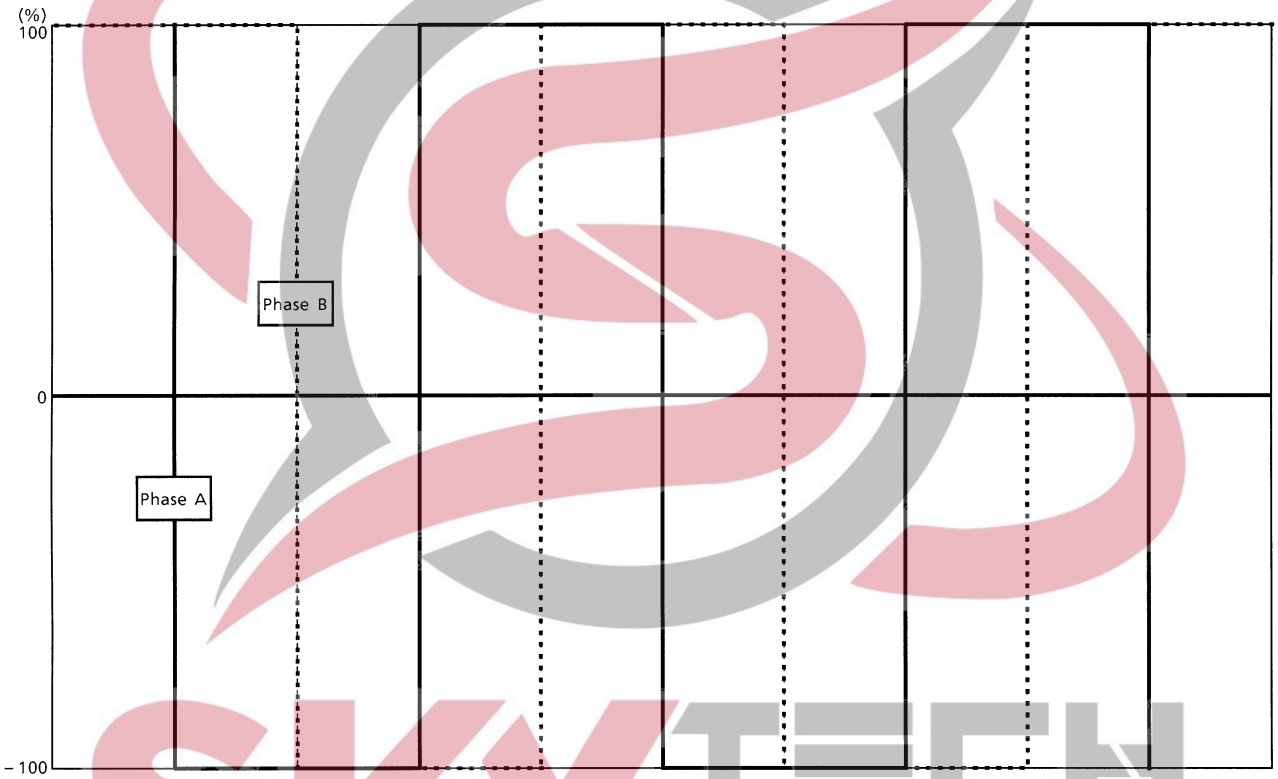
Therefore, from the time overcurrent flows to the output transistors to the time output halts is as follows.
Note that ideally, the operating time is the operating time when overcurrent flows. Depending on the output control mode timing, the overcurrent protector circuit may not be triggered.
Therefore, to ensure safe operation, add a fuse to the V_M power supply for protection.
The fuse capacity would vary according to the use conditions. However, select a fuse whose capacity avoids any operating problems and does not exceed the power dissipation for the IC.

Application Operation Input Data (Example: 2-Phase Excitation Mode)

	TORQUE 0	TORQUE 1	DECAY B_0	DECAY B_1	B_0	B_1	B_2	B_3	PHASE B	DECAY A	DECAY A_0	A_0	A_1	A_2	A_3	PHASE A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1
2	1	1	1	0	1	1	1	1	0	1	0	1	1	1	1	1
3	1	1	1	0	1	1	1	1	0	1	0	1	1	1	1	0
4	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) requires input of the Strobe signal.
For the input conditions, see page 9, Functions.
We recommend Mixed Decay mode (37.5%) as Decay mode. Set torque to 100%.

Output current waveform of 2-phase excitation sine wave



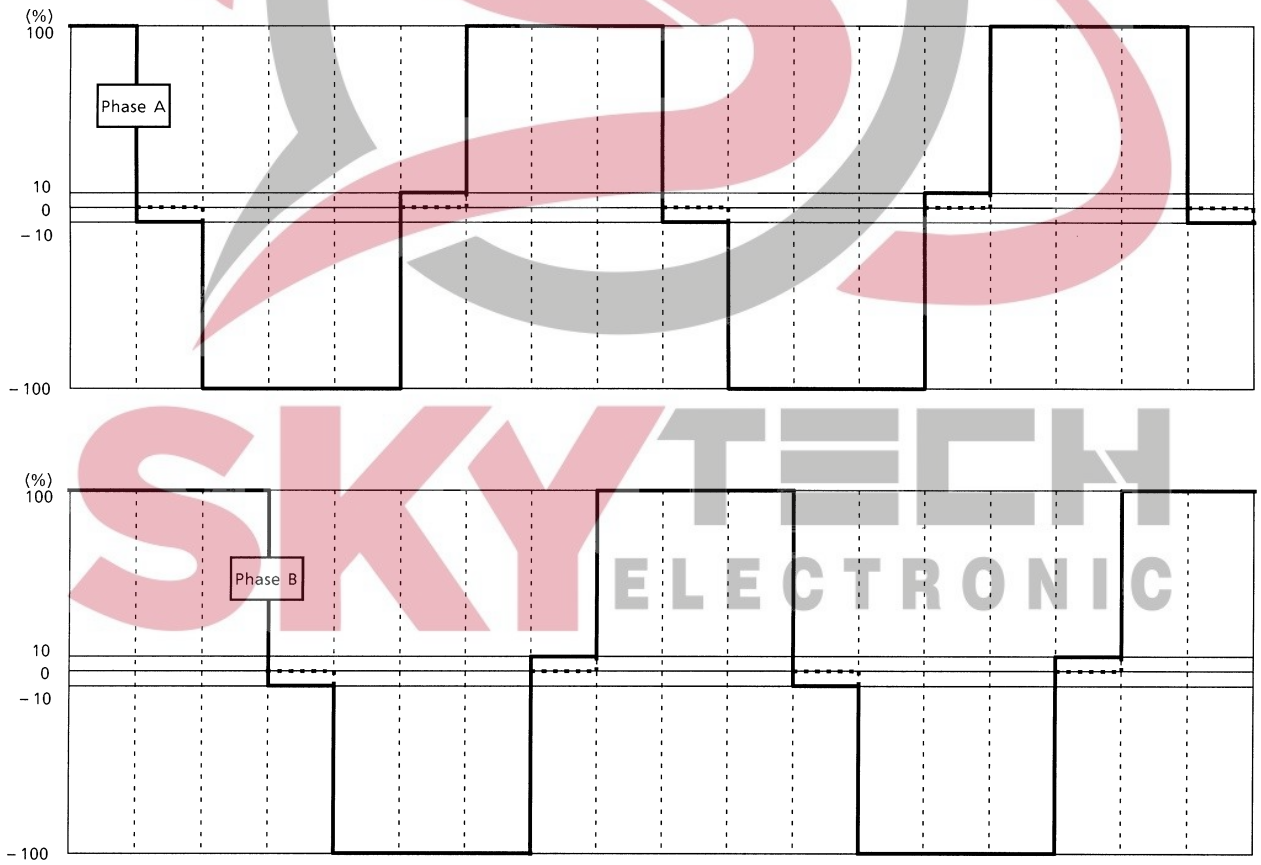
Note: We recommended 2-phase excitation drive in 37.5% Mixed Decay mode.
Please refer to the caution of 2-phase excitation mode on next page.

Application Operation Input Data (Example: 1-2 Phase Excitation Mode Typ.A)

	TORQUE 0	TORQUE 1	DECAY B_0	DECAY B_1	B_0	B_1	B_2	B_3	PHASE B	DECAY A_0	DECAY A_1	A_0	A_1	A_2	A_3	PHASE A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1
2	1	1	1	0	1	0	0	0	1	1	0	1	1	1	1	1
3	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1
4	1	1	1	0	1	1	1	1	0	1	0	1	0	0	0	0
5	1	1	1	0	1	1	1	1	0	1	0	1	1	1	1	0
6	1	1	1	0	1	0	0	0	0	1	0	1	1	1	1	0
7	1	1	1	0	1	1	1	1	0	1	0	1	1	1	1	0
8	1	1	1	0	1	1	1	1	1	1	0	1	0	0	0	1

Data are input on the rising edge of CLK. Every input of a data string (16-bit) requires input of the Strobe signal.
For the input conditions, see page 10, Functions.
We recommend Mixed Decay Mode (37.5%) as Decay Mode.
Set torque to 100%.
When using this excitation mode, high efficiency can be achieved by setting the phase data to 10% (–10%). Set current values in the order +100% → –10% → –100% → +10%.

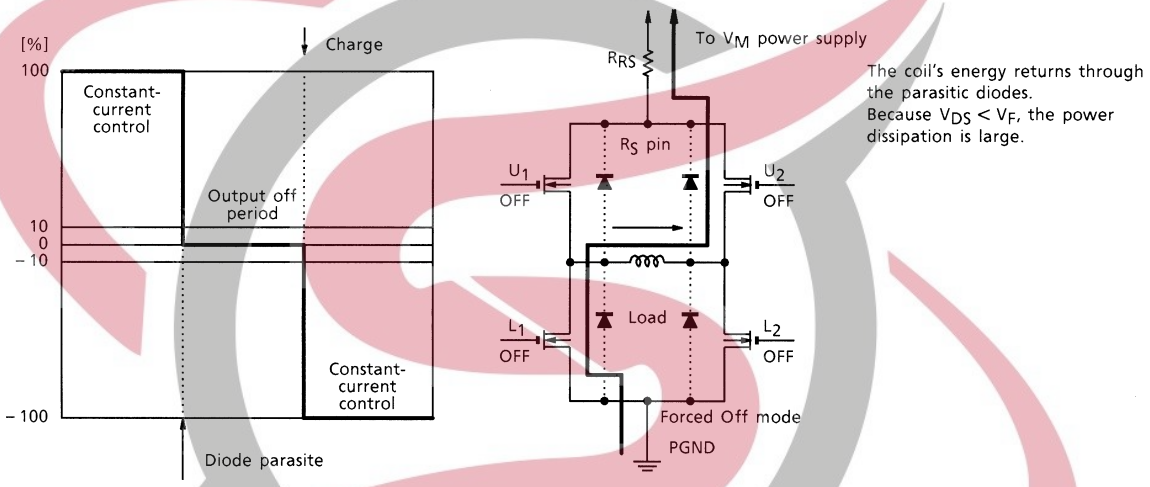
Output Current Waveform of 1-2 Phase Excitation Sine Wave (Typ. A)



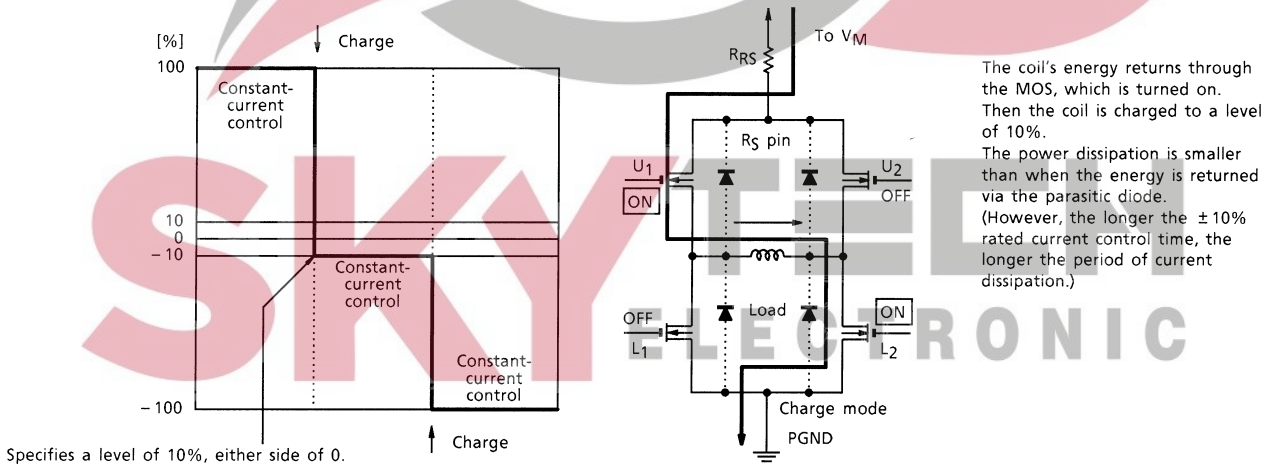
Points for Control that Includes Current of 0%

In modes other than 2-Phase Excitation mode (from 1-2 Phase Excitation mode to 4W1-2 Phase Excitation mode), when the current is controlled to 0%, the TB62201F's output transistors are all turned off.
At the time, the coil's energy returns to the power supply through the parasitic diodes. If the same current is applied several times and is within the rated current, then : the power consumed by the on-resistance when current flows to the output MOS will be less than the power consumed when current is applied to the parasitic diodes.
Therefore, when controlling the current, rather than setting 0%, set the current to the next step beyond 0% (the minimum step in the reverse direction) for better power dissipation results.
However, if the 0% (actually 10%) current cycle is long, the power dissipation may be greater than in Off mode because of the need for constant-current control.
Therefore, Toshiba recommend setting the current according to the actual operating pattern. (1-2 Phase Excitation mode is the most effective.)

Flyback diode mode



Non-flyback diode mode

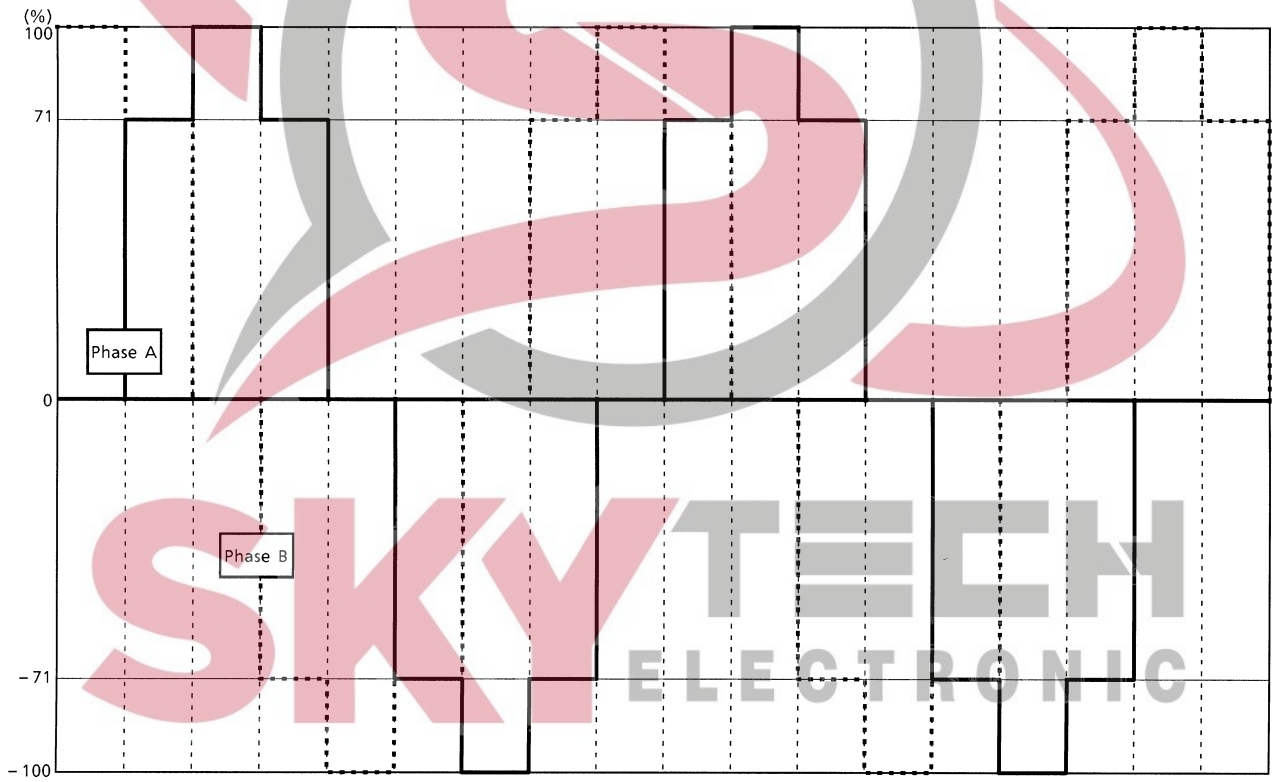


Application Operation Input Data (Example: 1-2 Phase Excitation mode Typ.B)

	TORQUE 0	TORQUE 1	MDMB	DECAY B	B_0	B_1	B_2	B_3	PHASE B	MDM A	DECAY A	A_0	A_1	A_2	A_3	PHASE A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1
2	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	1
3	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1
4	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	1
5	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	0
6	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0
7	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) requires input of the Strobe signal.
For the input conditions, see page 10, Functions.
We recommend Mixed Decay Mode (37.5%) as Decay Mode.
Set torque to 100%. Same as 1-2 phase excitation (typ. A) in the previous section, power dissipation can be reduced by changing 0% level to 10% or −10%.

Output Current Waveform of 1-2 Phase Excitation Sine Wave (Typ. B)

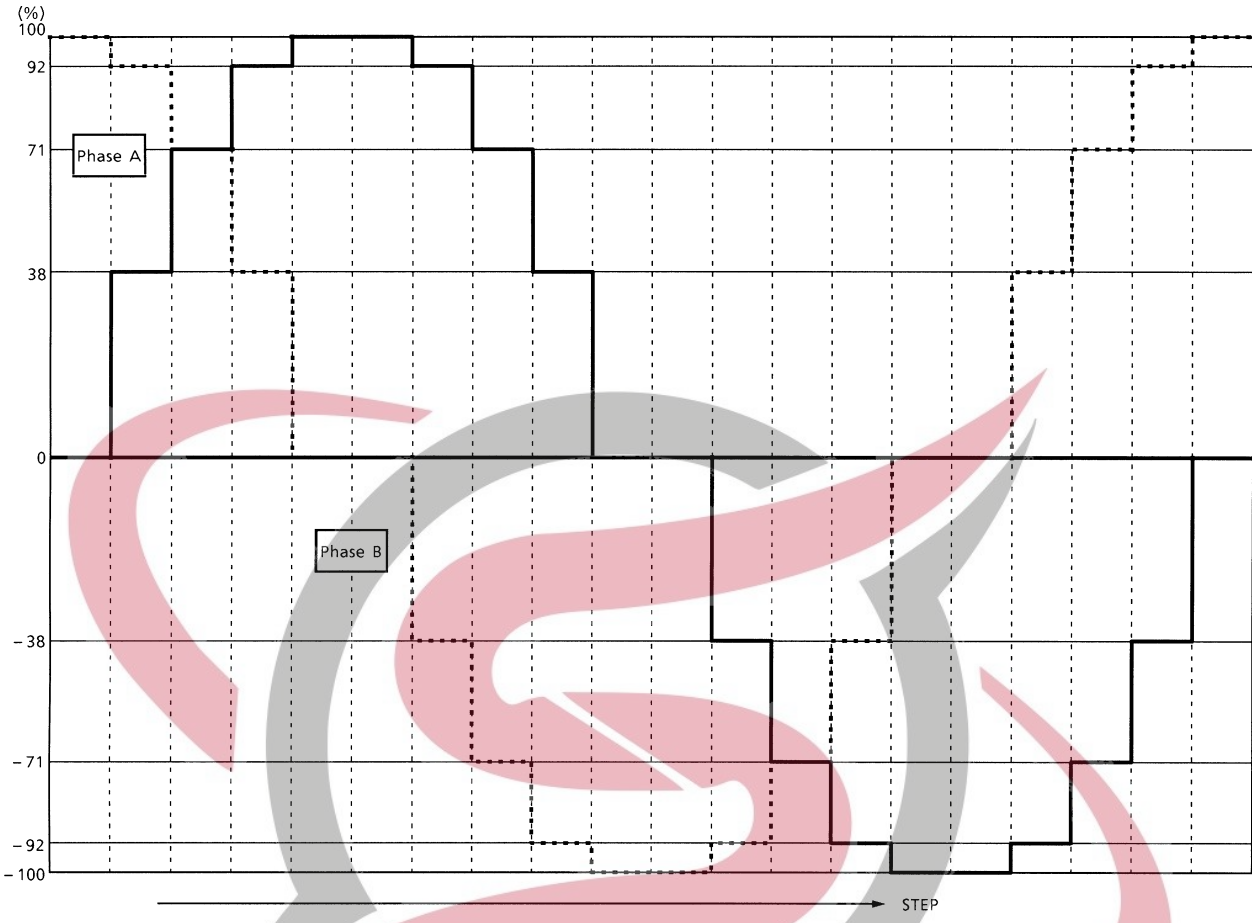


Application Operation Input Data (Example: 4-bit micro steps) (4-bit micro steps = W1-2 phase excitation drive)

	TORQUE 0	TORQUE 1	DECAY B_0	DECAY B_1	B_0	B_1	B_2	B_3	PHASE B	DECAY A_0	DECAY A_1	A_0	A_1	A_2	A_3	PHASE A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1
2	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	1
3	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	1
4	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	1
5	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1
6	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	1
7	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	1
8	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	1
9	1	1	1	0	0	0	1	1	0	1	0	0	0	1	0	1
10	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1
11	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0
12	1	1	1	0	0	0	1	1	0	1	1	0	0	1	0	0
13	1	1	1	0	0	0	0	1	0	1	1	0	0	0	1	0
14	1	1	1	0	0	0	1	0	0	1	1	0	0	1	1	0
15	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0
16	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	0
17	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	0
18	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	0
19	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	0
20	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) requires input of the Strobe signal. For the input conditions, see page 9, Functions.
We recommend Slow Decay Mode in the ascending direction of the sine wave ; Mixed Decay Mode (37.5%) in the descending direction. Set torque to 100%.

Output Current Waveform of Pseudo Sine Wave (4-bit micro steps)



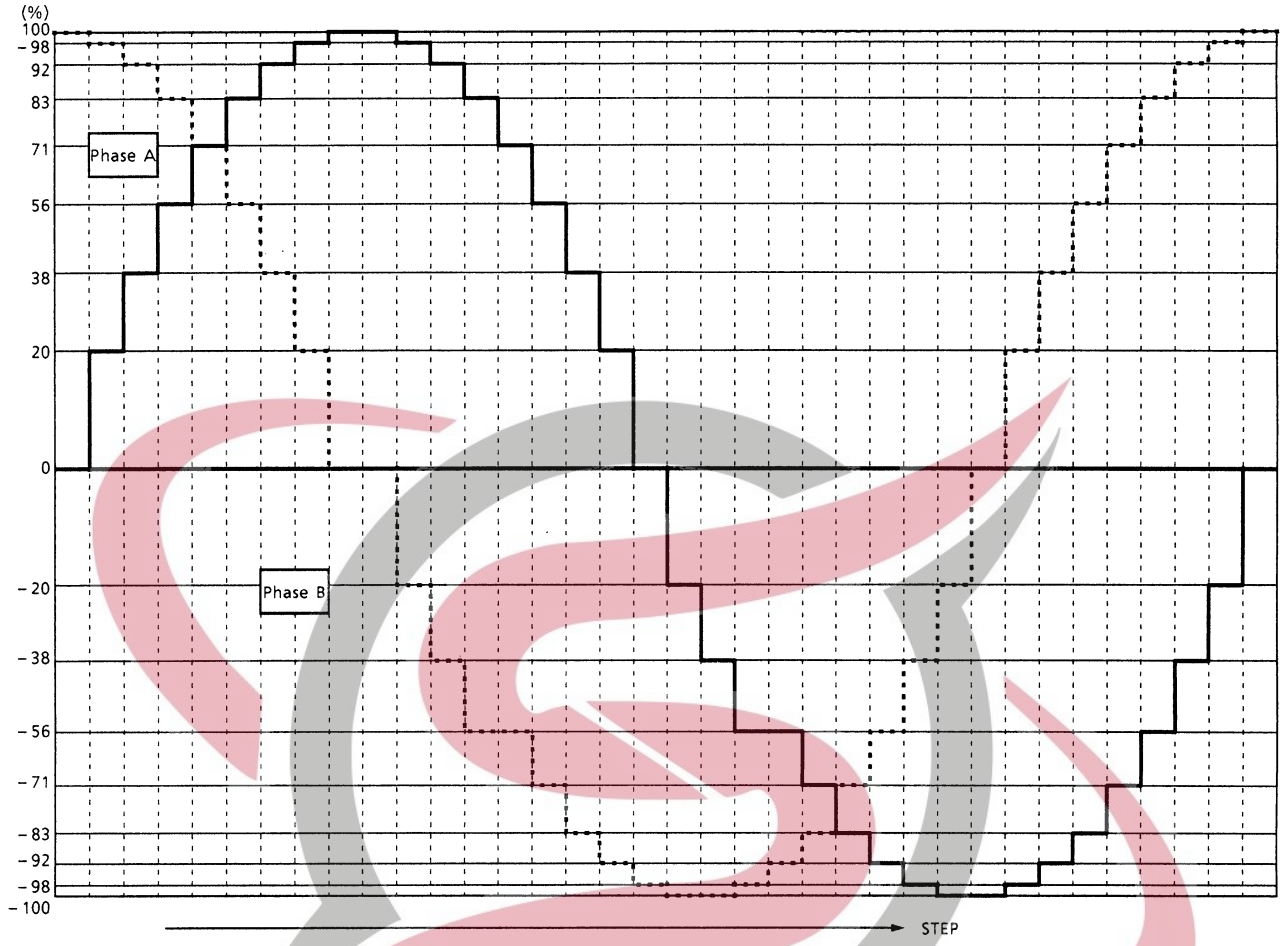
5 micro-step from 0 to 90° drive is possible by combining Current DATA (AB & CD) and phase data.
For input Current DATA at that time, see section on Current X in the list of the Functions.
Depending on the load, the optimum condition changes for selecting MIXED DECAY MODE when the sine wave rises and falls. Select the appropriate MIXED DECAY TIMING according to the load.

Application Operation Input Data (Example: 3-bit micro steps) (3-bit micro steps = 2W1-2 phase excitation drive)

	TORQUE 0	TORQUE 1	DECAY B_0	DECAY B_1	B_0	B_1	B_2	B_3	PHASE B	DECAY A_0	DECAY A_1	A_0	A_1	A_2	A_3	PHASE A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1
2	1	1	1	0	0	1	1	1	1	1	0	0	1	0	0	1
3	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	1
4	1	1	1	0	0	1	0	1	1	1	0	0	1	1	0	1
5	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	1
6	1	1	1	0	0	1	1	0	1	1	0	0	1	0	1	1
7	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	1
8	1	1	1	0	0	1	0	0	1	1	0	0	1	1	1	1
9	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1
10	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	1
11	1	1	1	0	0	1	0	0	0	1	0	0	1	1	1	1
12	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	1
13	1	1	1	0	0	1	1	0	0	1	0	0	1	0	1	1
14	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	1
15	1	1	1	0	0	1	0	1	0	1	0	0	1	1	0	1
16	1	1	1	0	0	0	1	1	0	1	0	0	0	1	0	1
17	1	1	1	0	0	1	1	1	0	1	0	0	1	0	0	1
18	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1
19	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0
20	1	1	1	0	0	1	1	1	0	1	1	0	1	0	0	0
21	1	1	1	0	0	0	1	1	0	1	1	0	0	1	0	0
22	1	1	1	0	0	1	0	1	0	1	1	0	1	1	0	0
23	1	1	1	0	0	0	0	1	0	1	1	0	0	0	1	0
24	1	1	1	0	0	1	1	0	0	1	1	0	1	0	1	0
25	1	1	1	0	0	0	1	0	0	1	1	0	0	1	1	0
26	1	1	1	0	0	1	0	0	0	1	1	0	1	1	1	0
27	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0
28	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	0
29	1	1	1	0	0	1	0	0	1	1	0	0	1	1	1	0
30	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	0
31	1	1	1	0	0	1	1	0	1	1	0	0	1	0	1	0
32	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	0
33	1	1	1	0	0	1	0	1	1	1	0	0	1	1	0	0
34	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	0
35	1	1	1	0	0	1	1	1	1	1	0	0	1	0	0	0
36	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) requires input of the Strobe signal. For the input conditions, see page 10, Functions.
We recommend Slow Decay Mode in the ascending direction of the sine wave; Mixed Decay Mode (37.5%) in the descending direction. Set torque to 100%.

Output Current Waveform of Pseudo Sine Wave (3-bit micro steps)



9 micro-step from 0 to 90° drive is possible by combining Current DATA (AB & CD) and phase data.
For input Current DATA at that time, see section on Current X in the list of the Functions.
Depending on the load, the optimum condition changes for selecting MIXED DECAY MODE when the sine wave rises and falls. Select the appropriate MIXED DECAY TIMING according to the load.

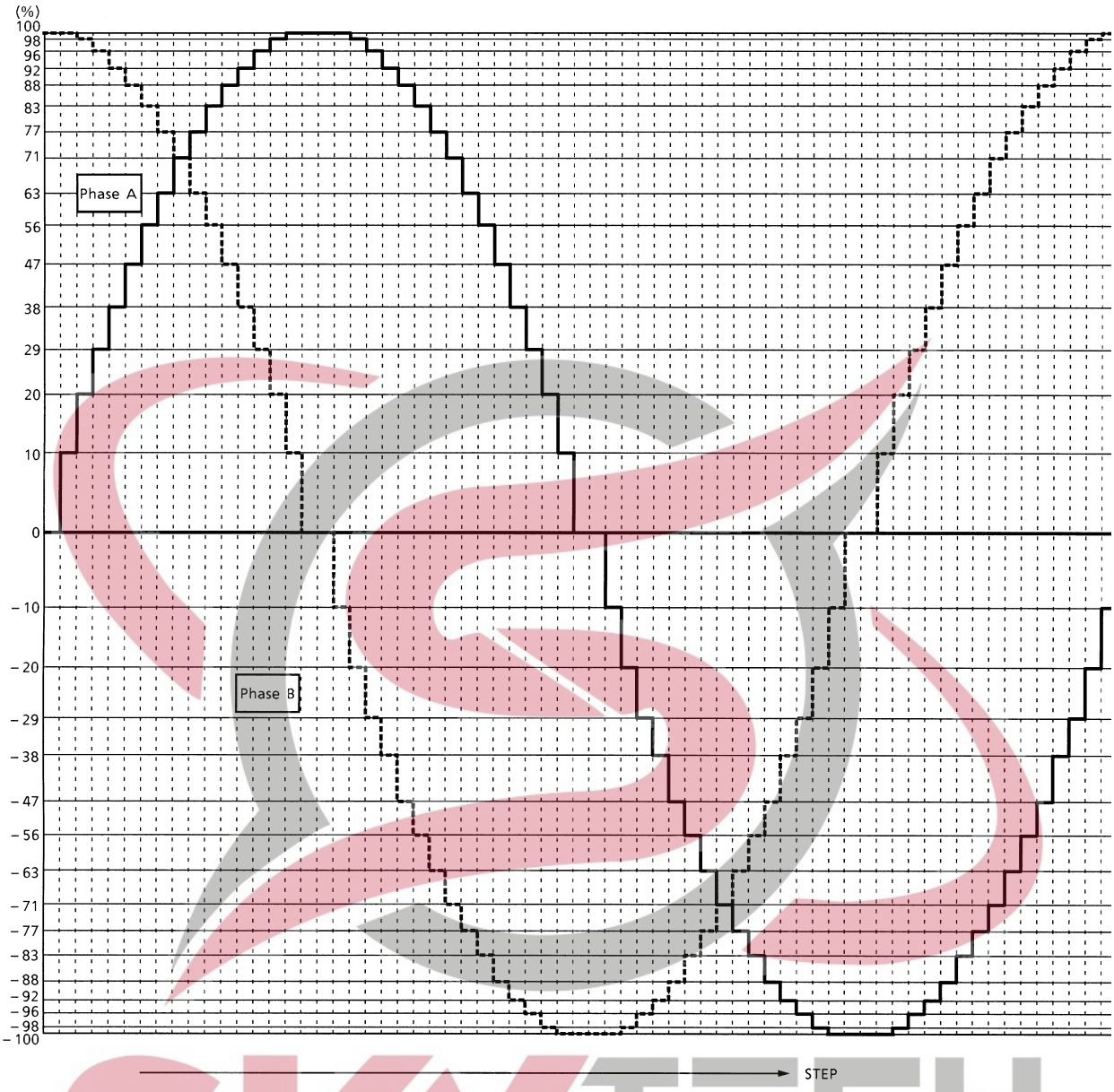
Application Operation Input Data (Example: 4-bit micro steps)

	TORQUE 0	TORQUE 1	DECAY B_0	DECAY B_1	B_0	B_1	B_2	B_3	PHASE B	DECAY A_0	DECAY A_1	A_0	A_1	A_2	A_3	PHASE A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1
2	1	1	1	0	1	1	1	1	1	1	0	1	0	0	0	1
3	1	1	1	0	0	1	1	1	1	1	0	0	1	0	0	1
4	1	1	1	0	1	0	1	1	1	1	0	1	1	0	0	1
5	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	1
6	1	1	1	0	1	1	0	1	1	1	0	1	0	1	0	1
7	1	1	1	0	0	1	0	1	1	1	0	0	1	1	0	1
8	1	1	1	0	1	0	0	1	1	1	0	1	1	1	0	1
9	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	1
10	1	1	1	0	1	1	1	0	1	1	0	1	0	0	1	1
11	1	1	1	0	0	1	1	0	1	1	0	0	1	0	1	1
12	1	1	1	0	1	0	1	0	1	1	0	1	1	0	1	1
13	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	1
14	1	1	1	0	1	1	0	0	1	1	0	1	0	1	1	1
15	1	1	1	0	0	1	0	0	1	1	0	0	1	1	1	1
16	1	1	1	0	1	0	0	0	1	1	0	1	1	1	1	1
17	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1
18	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	1
19	1	1	1	0	1	0	0	0	0	1	0	1	1	1	1	1
20	1	1	1	0	0	1	0	0	0	1	0	0	1	1	1	1
21	1	1	1	0	1	1	0	0	0	1	0	1	0	1	1	1
22	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	1
23	1	1	1	0	1	0	1	0	0	1	0	1	1	0	1	1
24	1	1	1	0	0	1	1	0	0	1	0	0	1	0	1	1
25	1	1	1	0	1	1	1	0	0	1	0	1	0	0	1	1
26	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	1
27	1	1	1	0	1	0	0	1	0	1	0	1	1	1	0	1
28	1	1	1	0	0	1	0	1	0	1	0	0	1	1	0	1
29	1	1	1	0	1	1	0	1	0	1	0	1	0	1	0	1
30	1	1	1	0	0	0	1	1	0	1	0	0	0	1	0	1
31	1	1	1	0	1	0	1	1	0	1	0	1	1	0	0	1
32	1	1	1	0	0	1	1	1	0	1	0	0	1	0	0	1
33	1	1	1	0	1	1	1	1	0	1	0	1	0	0	0	1
34	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1

	TORQUE 0	TORQUE 1	DECAY B_0	DECAY B_1	B_0	B_1	B_2	B_3	PHASE B	DECAY A_0	DECAY A_1	A_0	A_1	A_2	A_3	PHASE A
Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
35	1	1	1	0	1	1	1	1	0	1	1	0	0	0	0	0
36	1	1	1	0	1	1	1	1	0	1	1	1	0	0	0	0
37	1	1	1	0	0	1	1	1	0	1	1	0	1	0	0	0
38	1	1	1	0	1	0	1	1	0	1	1	1	1	0	0	0
39	1	1	1	0	0	0	1	1	0	1	1	0	0	1	0	0
40	1	1	1	0	1	1	0	1	0	1	1	1	0	1	0	0
41	1	1	1	0	0	1	0	1	0	1	1	0	1	1	0	0
42	1	1	1	0	1	0	0	1	0	1	1	1	1	1	0	0
43	1	1	1	0	0	0	0	1	0	1	1	0	0	0	1	0
44	1	1	1	0	1	1	1	0	0	1	1	1	0	0	1	0
45	1	1	1	0	0	1	1	0	0	1	1	0	1	0	1	0
46	1	1	1	0	1	0	1	0	0	1	1	1	1	0	1	0
47	1	1	1	0	0	0	1	0	0	1	1	0	0	1	1	0
48	1	1	1	0	1	1	0	0	0	1	1	1	0	1	1	0
49	1	1	1	0	0	1	0	0	0	1	1	0	1	1	1	0
50	1	1	1	0	1	0	0	0	0	1	1	1	1	1	1	0
51	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0
52	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	0
53	1	1	1	0	1	0	0	0	1	1	0	1	1	1	1	0
54	1	1	1	0	0	1	0	0	1	1	0	0	1	1	1	0
55	1	1	1	0	1	1	0	0	1	1	0	1	0	1	1	0
56	1	1	1	0	0	0	1	0	1	1	0	0	0	1	1	0
57	1	1	1	0	1	0	1	0	1	1	0	1	1	0	1	0
58	1	1	1	0	0	1	1	0	1	1	0	0	1	0	1	0
59	1	1	1	0	1	1	1	0	1	1	0	1	0	0	1	0
60	1	1	1	0	0	0	0	1	1	1	0	0	0	0	1	0
61	1	1	1	0	1	0	0	1	1	1	0	1	1	1	0	0
62	1	1	1	0	0	1	0	1	1	1	0	0	1	1	0	0
63	1	1	1	0	1	1	0	1	1	1	0	1	0	1	0	0
64	1	1	1	0	0	0	1	1	1	1	0	0	0	1	0	0
65	1	1	1	0	1	0	1	1	1	1	0	1	1	0	0	0
66	1	1	1	0	0	1	1	1	1	1	0	0	1	0	0	0
67	1	1	1	0	1	1	1	1	1	1	0	1	0	0	0	0
68	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0

Data are input on the rising edge of CLK. Every input of a data string (16-bit) requires input of the Strobe signal. For the input conditions, see page 10, Functions. In the above input data example, Decay mode has a Mixed Decay mode (37.5%) setting for both the rising and falling directions of the sine wave, and a torque setting of 100%.

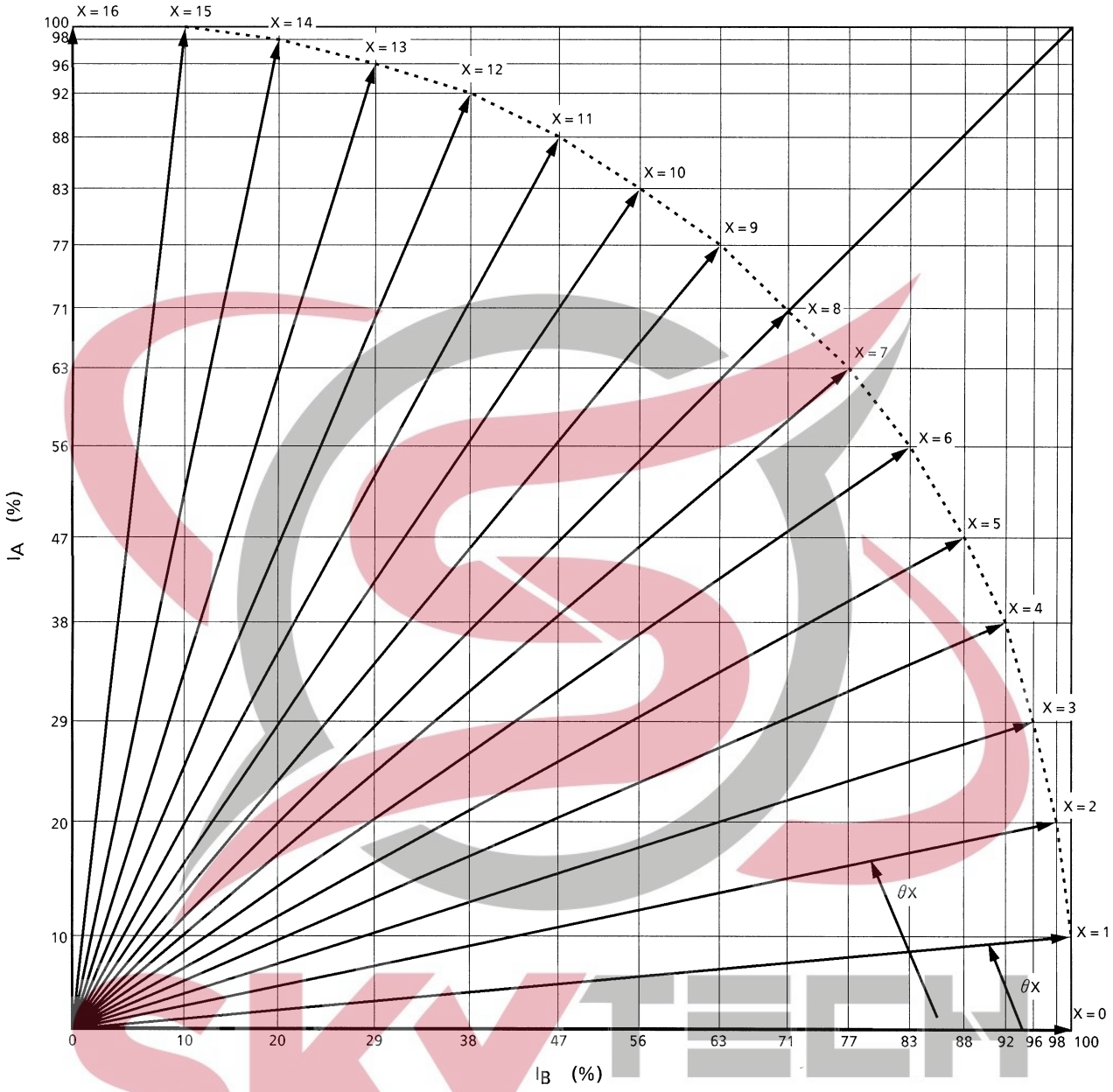
4W1-2 Output Current Waveform of Pseudo Sine Wave (4-bit micro steps)



17 micro-step from 0 to 90° drive is possible by combining Current DATA (AB & CD) and phase data.
For input Current DATA at that time, see section on Current X in the list of the Functions.
Depending on the load, the optimum condition changes for selecting MIXED DECAY MODE when the sine wave rises and falls. Select the appropriate MIXED DECAY TIMING according to the load.

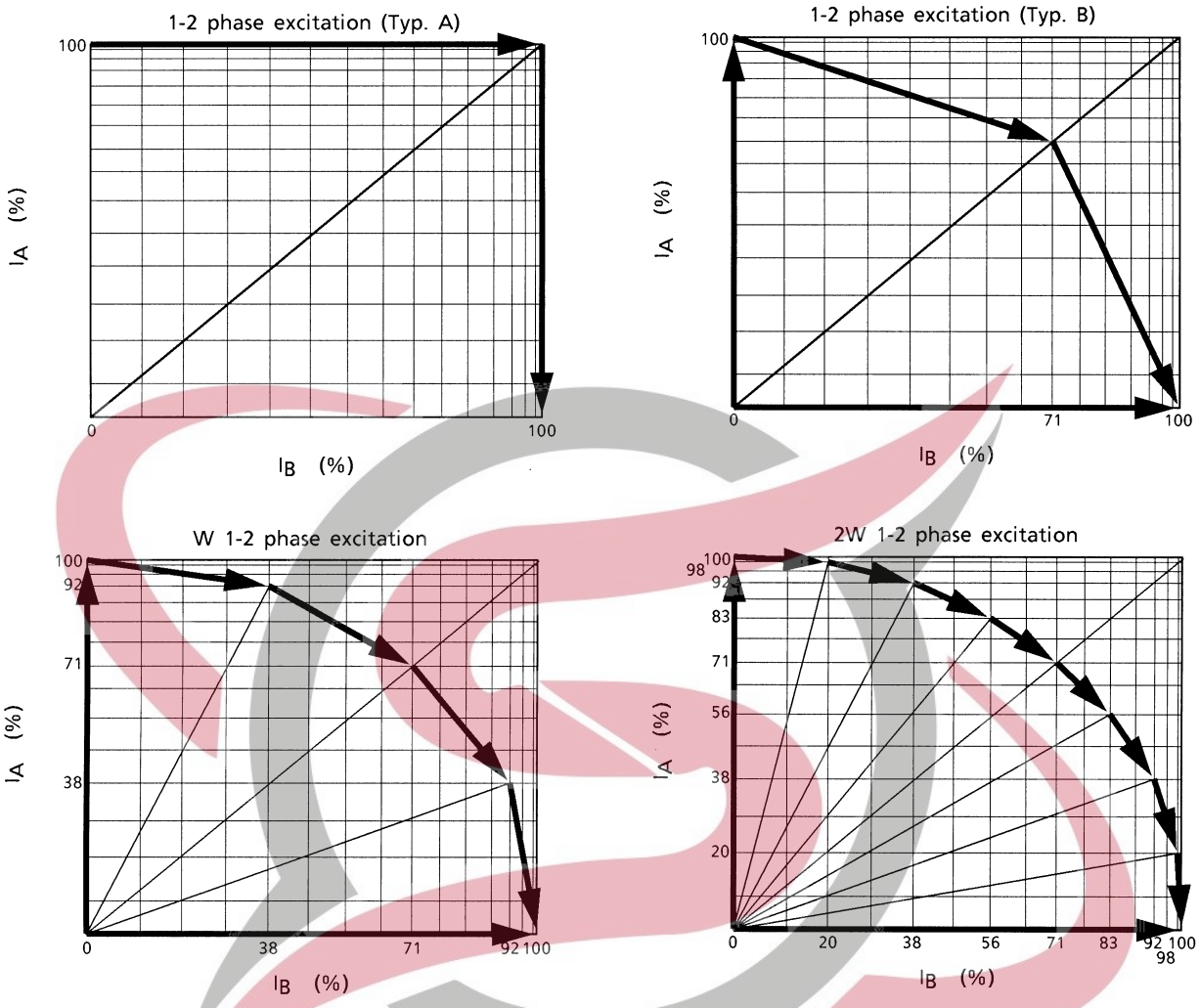
Output Current Vector Line

4W-1-2 phase excitation (4-bit micro steps)



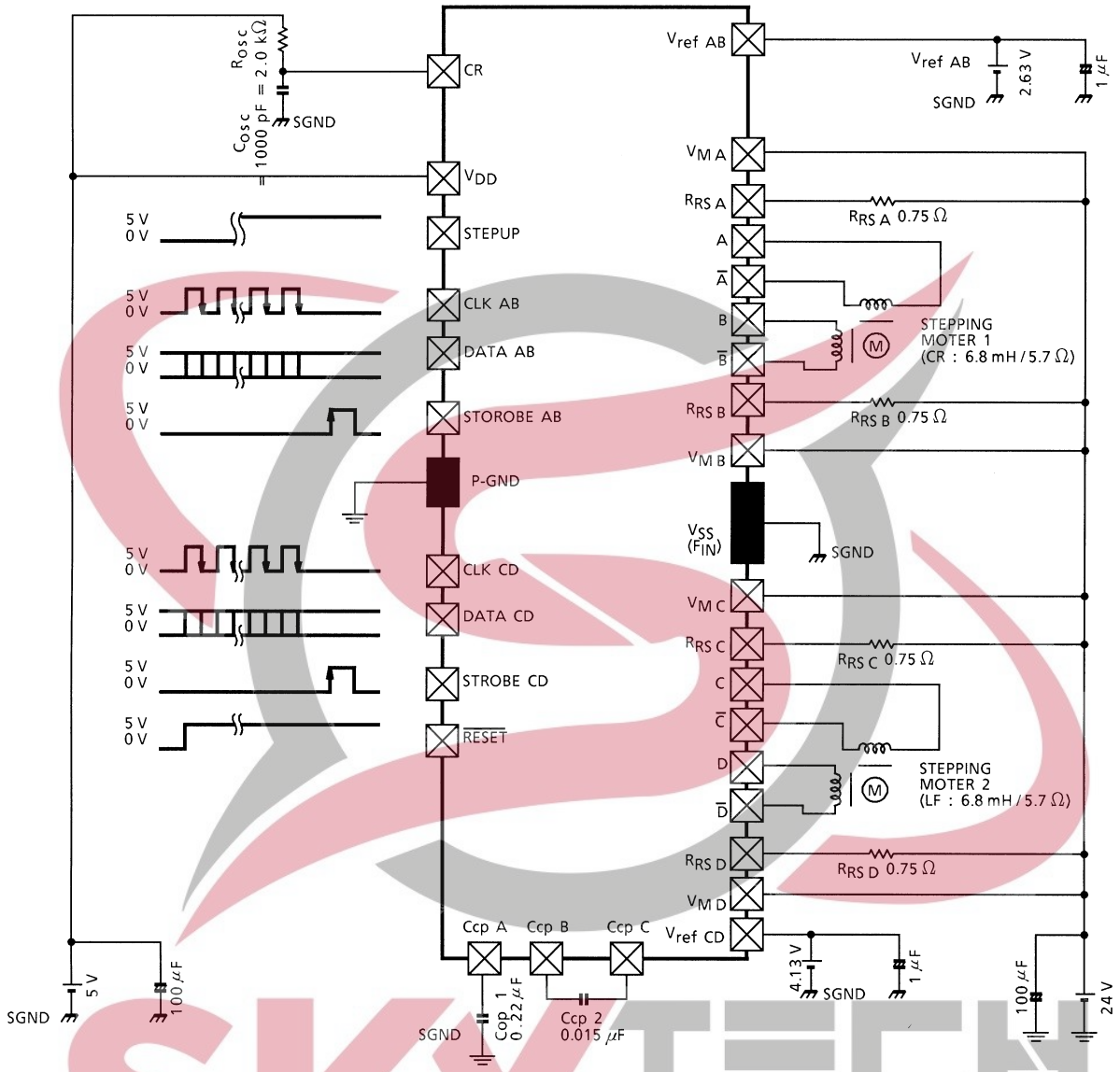
For data to be input, see the function of Current AX (BX) in the list of Functions (10 page).

Output Current Vector Line 2 (Each mode: except 4W1-2 phase)



Recommended Application Circuit

The values for the devices are all recommended values. For values under each input condition, see the above-mentioned recommended operating conditions.
(Example : f_{chop} = 96 kHz, CR : I_{out} = 0.6 (A), LF : I_{out} = 0.6 (A))



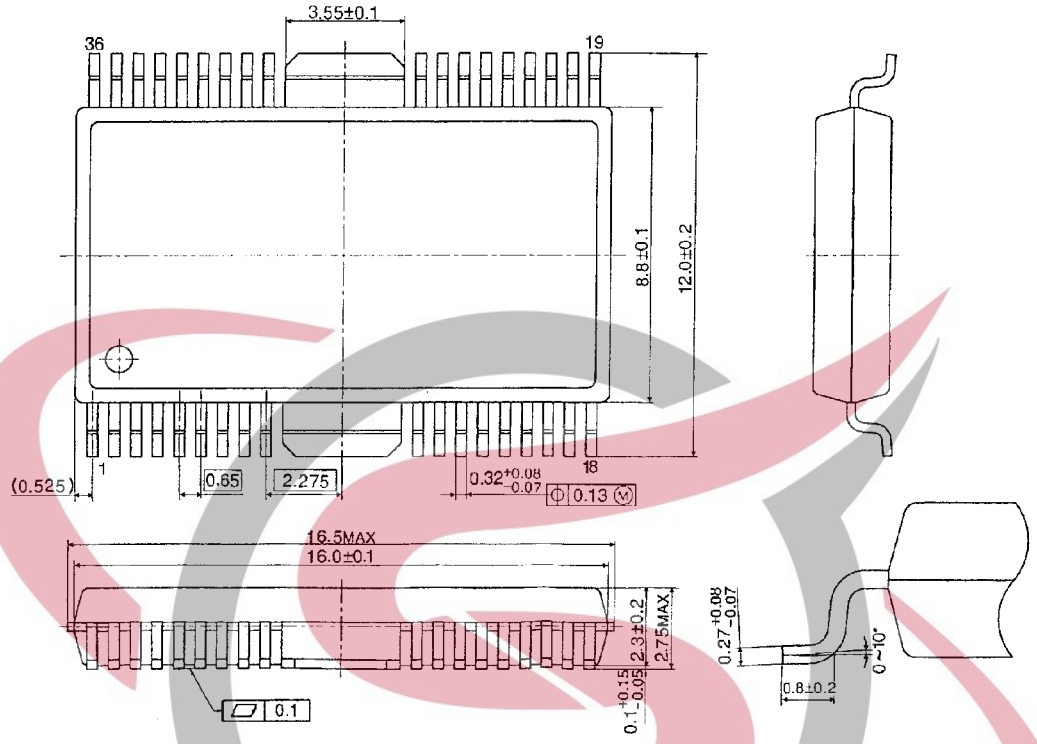
Note: We recommend the user add bypass capacitors as required.
Make sure as much as possible that GND wiring has only one contact point.
Also, make sure that the VM pins are connected.

For the data to be input, see the section on the recommended input data.

Because there may be shorts between outputs, shorts to supply, or shorts to ground, be careful when designing output lines, V_{DD} (V_M) lines, and GND lines.

Package Dimensions

HSOP36-P-450-0.65 Unit: mm



Weight: 079 g (typ.)

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030619EBA

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